Testing and Validation of Phasor Measurement Based Devices and Algorithms

Final Project Report

Power Systems Engineering Research Center

Empowering Minds to Engineer
the Future Electric Energy System

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Power Systems Engineering Research Center

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Executive Summary

For upgrading the traditional electric power system to a smart power grid, it is essential to make several enhancements at various levels of operation and control, which includes the integration of Intelligent Electronic Devices (IEDs), synchrophasor devices, advanced communication infrastructure and efficient monitoring and controlling algorithms that would make optimum use of these devices. The event of August 14, 2003 blackout in the north eastern United States and parts of Canada that affected almost 50 million people emphasized the need for real time situational awareness, and thus advocated the use of synchrophasor devices in the power system. PMUs enable the wide area visualization of a power system in real time by capturing high speed time-stamped snapshots in the form of voltage and current phasors, frequency and rate of change of frequency at the rate of up to 120 frames/second. This kind of "time stamping" allows the measurements from different geographical locations to be time-aligned or "synchronized", thus providing a precise and comprehensive view of the entire system. Synchrophasor technology enables a good indication of the status or condition of power grid in real time. However, before putting the smart devices and algorithms in use in the actual power grid, it is of utmost importance to test and validate their capabilities as well as their accuracy.

The motive is to ensure high accuracy of measurements from synchrophasor devices and the validation of developed algorithms utilizing synchrophasors, under different operating scenarios of the power system. This research project report mainly focuses on following goals, (a) testing and validation of synchrophasor devices; b) testing of phasor based voltage stability and state estimation applications utilizing a real time hardware-in-the-loop (HIL) test bed; and (c) utilization of PMUs for advanced protection schemes with emphasis on dynamic protection algorithms for transformers.

To achieve these goals, the testing facility based on Real Time Digital Simulator (RTDS) at Washington State University (WSU) and WinIGS-T at Georgia Institute of Technology (GIT) were both upgraded to perform testing of synchrophasor devices and applications. For synchrophasor device testing, test systems and also library of test conditions were developed to simulate system scenarios as specified in IEEE C37.118.1 standard. Testing for number of phasor measurement units (PMUs) have been performed against modeled standard PMU. Testing for software and hardware phasor data concentrators (PDCs) have been also performed against limited number of performance criterion. For real time testing and validation of phasor based applications, we focused on voltage stability, state estimators and dynamic protection algorithms for transformers. These applications were simulated in lab environment for some example algorithms to check performance and find potential problems before installing in industry grade power system.

Synchrophasor Device Testing

Test conditions for PMU's include a) nominal and off-nominal frequency; and b) with and without harmonics, under balanced steady state conditions while magnitude, phase angle and frequency are changed within ranges as specified in the IEEE C37.118.1 standard. For dynamic testing, test conditions include, a) magnitude, angle and frequency

step change; b) frequency ramp change; and c) amplitude, phase and frequency modulation.

The tests reveal that the performance of the different PMUs tested in lab are excellent under steady state conditions and near nominal frequency. The tested PMUs meet the IEEE Standard permissible error of total vector error. However under dynamic and off nominal frequency there is great variability among the various manufacturers and the errors can be quite high. All performance data do not identify the specific device tested. Also, total vector error (TVE) for current is generally higher than voltage TVE and TVE is not the same for each phase. Frequency error (FE) and rate of change in frequency (ROCOF) error (RFE) is within limits for most of the cases. For dynamic testing example of one specific PMU, magnitude step change and angle step change meets the requirement of response time and peak overshoot but not the delay time. For frequency step change, requirements for frequency response time and peak overshoot are met but not the ROCOF response time and delay time. For, frequency ramp change, requirements are not met for FE and RFE. For, amplitude phase and frequency modulation test, PMU fails all performance criterion testing.

Test results for PDC show that the tested PDCs shows satisfactory response in aligning data and data validation test was also successful for different durations and reporting rate of data streaming, collection and archival. There is no data loss, if PMU directly streams data to a PDC without going through a complex communication network. However, when the PMU sends data to the PDC via communication networks, there is considerable data loss. Data latency, data rate conversion, format conversion, phase/ magnitude compensation were found satisfactory for tested PDC's.

Synchrophasor Application Testing

The test bed was modified to perform real time testing of voltage stability algorithms using real time controllers and real time digital simulators. Voltage stability algorithm tested in lab shows performance as expected for line outages and change in loading conditions. State estimation algorithm is dynamic and perform very well with transformer inrush current, over-excitation and with fault conditions.

The setting-less protection approach based on dynamic state estimation for the 3-phase transformer has been proven to be a reliable method to protect the transformer against internal faults. It was shown that the relay does not trip during normal operating conditions or faults outside the protection zone. On the other hand, a trip is decided during the internal fault. The simulation results verify the theoretical analysis. The computation time needed is within the requirements of the data acquisition scheme.

Outcomes of this project include (a) Set of standard accuracy and performance tests for PMUs; (b) An enhanced test bed to demonstrate operation of phasor devices for research/ educational purposes; (c) Evaluation of PMU based applications including voltage stability and state estimation in real time; and (d) Better dynamic protection algorithm for transformer.

Performance results reported here for PMU and PDC can be used to guide evolution of the standards and to provide insight for manufacturer. Test results also shows need for additional algorithms to filter out bad data for applications related to transients and dynamics as well as real time control. Dynamic protection algorithms for transformer protection can be incorporated in new relays with PMU capability.

Project Publications:

[1]. Saugata S. Biswas, Jeong Hun Kim and Anurag K. Srivastava, "Development of a Smart Grid Test bed and Applications in PMU and PDC Testing," in *North American Power Symposium (NAPS), Urbana, IL*, September 2012.

[2]. Saugata S. Biswas and Anurag K. Srivastava, "Real time Testing and Validation of Smart Grid Devices and Algorithms," in *IEEE PES General Meeting*, Vancouver, CA, July 2013.

[3]. Saugata S. Biswas and Anurag K Srivastava, "A Novel Method for Distributed Real Time Voltage Stability Monitoring Using Synchrophasor Measurements", IREP Symposium, Rethymnon, Crete, Greece, June 2013.

[4]. Saugata S Biswas and Anurag K Srivastava, "A fast Algorithm for Voltage Stability Monitoring of Power Systems with Consideration of Load Models", IEEE IAS Meeting, Orlando, FL, October, 2013.

[5]. Saugata S. Biswas, Ceeman B. Vellaithurai and Anurag K. Srivastava, " Development and Real Time Implementation of a Synchrophasor based Fast Voltage Stability Monitoring Algorithm with Consideration of Load Models," submitted to IEEE Transactions for Industrial Applications.

[6]. Sakis Meliopoulos, George Cokkinides, Zhenyu Tan, Sungyun Choi, Yonghee Lee and Paul Myrda, "Setting-less Protection: Feasibility Study", proceedings of HICSS 2013, Maui, HI, January 2013

[7]. A. P. Meliopoulos, E. Polymeneas, Zhenyu Tan, Renke Huang, and Dongbo Zhao, "Advanced Distribution Management System", *IEEE Transactions on Smart Grid*, accepted.

[8]. Sakis Meliopoulos, G. J. Cokkinides, S. Grijalva, R. Huang, E. Polymeneas, Paul Myrda, Evangelos Farantatos, Mel Gehrs, "Integration & Automation: From Protection to Advanced Energy Management Systems", IREP Symposium, Rethymnon, Crete, Greece, June 2013.

Student Theses:

[1]. Saugata Biswas, Development and validation of real time monitoring and control algorithms for power system, Ph.D. thesis, Washington State University, May 2014.

[2]. Yonghee Lee, Comprehensive Protection Schemes of a Microgrid and Distribution Systems, Ph.D. thesis, Georgia Institute of Technology, in progress.

[3]. Stefan Ntwoku, Dynamic Transformer Protection: a Novel Approach Using State Estimation, Georgia Institute of Technology, August 2012.

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1. Introduction

1.1 Background

Implementation of the future smart grid requires adopting number of new technologies including integration of phasor based devices and new algorithms to utilize synchrophasor data for various applications. These newly developed phasor based applications need to be validated before actual implementation. In order to properly evaluate the applications, it is important to characterize the phasor measurement units (PMUs) and the quality of data obtained with the PMUs. Testing of phasor based devices including PMUs and phasor data concentrators (PDCs) for technical performance are required before installing in real world application. Utilities need to assure the reliable operation of PMUs with high data quality before they will invest heavily in them. PMU data quality is critical especially for control applications. The updated Synchrophasor standard IEEE C37.118.1-2011 (released in 2011) defines the requirements for the PMU measurements in terms of the steady state performance evaluation quantities like Total Vector Error (TVE), Frequency Error (FE) and Rate of change of Frequency Error (RFE), and dynamic evaluation quantities like peak overshoot, response time and delay time [1, 2]. The standard specifies test conditions that include various ranges of signal frequency, magnitude and phase angle, as well as levels of harmonic distortion. North American Synchro Phasor Initiative (NASPI) [3] has also addressed the issue of PMU testing to help with developing technical guidelines and educational documents. There are other parallel efforts by researchers, but PMU applications and devices have been evolving over the years and need to be tested with new developments.

1.2 Project Objectives and Overview

This research project mainly focuses on (a) testing of phasor devices like PMUs and PDCs; (b) testing and validation of phasor based voltage stability and state estimation applications utilizing an existing real time hardware-in-the-loop (HIL) test bed; and (c) utilization of PMUs for advanced protection schemes with emphasis on dynamic protection algorithms for transformers.

Two proposed test beds have been utilized, one based on the Real Time Digital Simulator (RTDS) at WSU [4, 5] and another based on a digital simulator (WinIGS-T) at GIT. Both test beds utilize additional hardware and software tools including Phasor Measurement Units (PMUs), amplifiers, Synchrophasor Vector Processor (SVP), Phasor Data Concentrators (PDC) and Historians.

Voltage stability and state estimation algorithms based on PMU data have been addressed in several publications but there is need for real time validation before implementation. Dynamic protection algorithms are in their infancy - yet they offer great promise to provide robust, reliable protection schemes for the most difficult protection problems. The use of PMUs for dynamic protection algorithms for transformer protection has been investigated in this project. Transformer protection is the best candidate to test dynamic

protection algorithms since inrush currents in transformers have been known to impose compromises in differential transformer protection. For instance, the many excellent schemes to deal with inrush currents in transformer protection: the algorithms and hardware for identifying inrush currents are not fully reliable or accurate and as a result the settings are normally desensitized, protection action is delayed and transformers are subjected to abnormal conditions longer than necessary. It is generally accepted that dynamic protection algorithms have the capacity to provide more robust, highly selective and reliable algorithms.

This project provides several potential benefits including (a) Better dynamic protection algorithm for transformer; (b) Set of standard accuracy and performance tests for PMUs and a guide for PMU real time applications resulting in cost reduction and verifiable operational performance; (c) An enhanced test bed to demonstrate operation of phasor devices for educational purposes; and (d) Evaluation of PMU based applications including voltage stability and state estimation in real time. Improved test bed can be used for educational/ research purpose.

1.3 Report Organization

This report has been organized in four sections. Section 1 provides introduction, project objectives and overview of the problem. Section 2 provides details for testing of phasor measurement devices and phasor data concentrator using the enhanced test bed at WSU and GIT. Section 3 presents test results for testing and validation of three different phasor applications for voltage stability, state estimation and dynamic protection. Section 4 concludes the report.

2. Synchrophasor Device Testing

2.1 RTDS Based Testing Facility

2.2.1 Description

Real Time Digital Simulator (RTDS) is a power system simulator that simulates a power system built in RSCAD user interface software in real time. The RTDS works on the parallel processing technology of digital signal processors and executes the program developed on its processors. The RTDS not only calculates and shows the electrical output values in the runtime software, but also produces scaled output signals (digital as well as analog) through the output interface cards incorporated into its system.

Figure 2.1: Test bed at Washington State University

The RTDS facility installed at the Smart Grid Demonstration & Research Investigation Lab (SGDRIL), WSU, consists of one rack with three Giga Processor Cards (GPCs) and two PB5 Cards for processing required computations in real time. Other components include: a) One Giga Transceiver Workstation Interface Card (GTWIF) – for interfacing the RSCAD user software with the GPC cards of the RTDS; b) one Giga Transceiver Digital Input Card (GTDI) – for taking in input digital signals from external devices like PMU/ relays; c) one Giga Transceiver Front Panel Interface card (GTFPI) – for taking in

input digital signals and giving out output digital signals from and to hardware devices like relays; d) three Giga Transceiver Analog Output Card (GTAO) – for providing analog output signals to hardware devices like PMUs for measuring electrical quantities; e) one Giga Transceiver Analog Input Card (GTAI) – for taking in analog input signals from hardware devices; f) one Giga Transceiver Network Interface Card (GTNET) – for interfacing a number of different network protocols with the RTDS simulator; and g) one Giga Transceiver Synchronization Card (GTSYNC) – for synchronizing the RTDS simulation time step to an external time reference like the GPS clock. Additionally, test bed consists of number of PMU devices, phasor data concentrators (PDCs), synchrophasor vector processors (SVP), controllers, and amplifiers. Fig. 2.1 shows the lab setup at WSU.

2.2.2 PMU Testing

2.1.2.1 Introduction

PMUs enable the wide area visualization of a power system in real time by capturing high speed time-stamped snapshots in the form of voltage and current phasors, frequency and rate of change of frequency at the rate of 30/60/120 Frames / second [6]. This kind of "time stamping" allows the measurements from different geographical locations to be time-aligned or "synchronized", thus providing a precise and comprehensive view of the entire system. Hence, synchrophasor technology enables a good indication of the status or condition of power grid in real time. However, before putting the smart devices and algorithms in use in the actual power grid, it is of utmost importance to test and validate their capabilities as well as their accuracy. The motive is to ensure high reliability and accuracy of these devices and the developed algorithms, under different operating scenarios of the power system.

2.1.2.2 Library of Test Conditions

IEEE Standard for Synchrophasors C37.118 - 2011 [7] is the latest standard that provide the PMU performance conformance test details. This Standard has been divided into two parts - C37.118.1 and C37.118.2, where the former specifies the tests required for PMU measurement performance conformance, while the latter specifies the tests required for PMU communication performance conformance. In this project, the PMU measurement performance tests have been performed (as mentioned in IEEE C37.118.1). Also additional tests that are not in the present standard have been performed, keeping in mind some of the realistic system conditions in which the PMUs are supposed to operate when deployed in substations. Thus, the specially designed test library performs a comprehensive performance analysis of the PMUs.
The 'library of test conditions' has been created in the RTDS using test case as shown in fig. 2.2. Individual test cases have been created in the RTDS Draft case so as to generate the test signals. The ideal PMU is the GTNET PMU available in the RTDS. The draft case is set up in such a way the test PMU is connected to the same bus as that of the GTNET PMU, so that both the PMUs get the same measurements as their inputs.

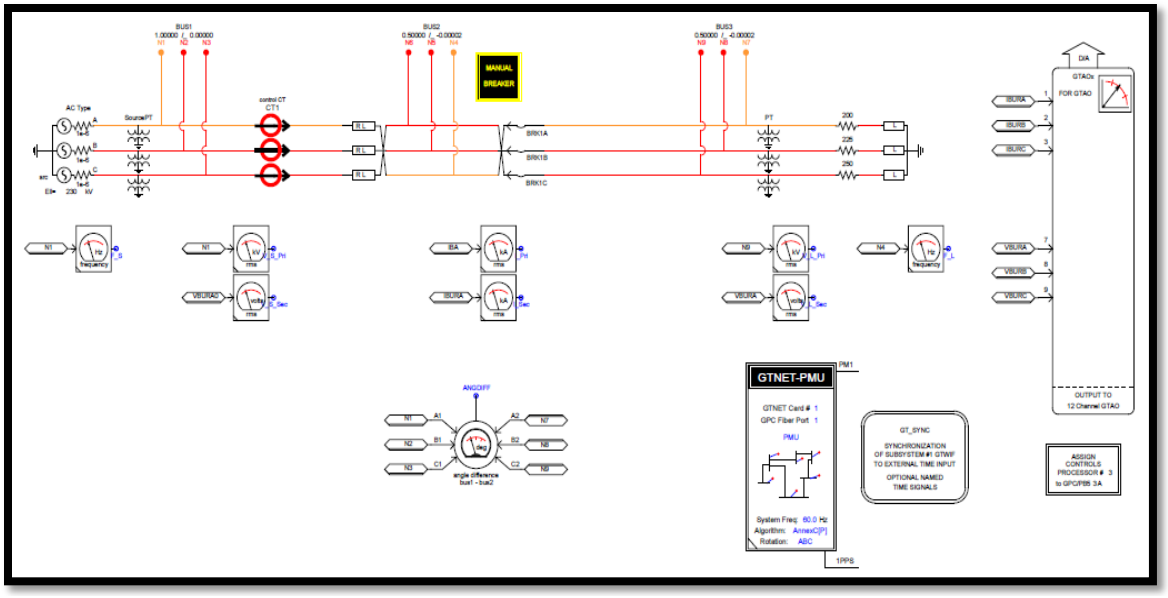

Figure 2.2: Example of a draft case for simulating a PMU test condition

Table 2.1: Library of test conditions for PMU testing

Main Category of PMU Testing	Quantities Changed during Testing	System Conditions during Testing	PMU Performance Evaluation Parameters
Steady State Tests	Voltage & Current Magnitude	System is balanced	TVE, FE, RFE
		System is at off-nominal frequency	TVE, FE, RFE
		System has harmonics	TVE, FE, RFE
		System is at off-nominal frequency and has harmonics	TVE, FE, RFE
	Voltage & Current Angle	System is balanced	TVE, FE, RFE
		System has harmonics	TVE, FE, RFE
	Frequency	System is balanced	TVE, FE, RFE
		System has harmonics	TVE, FE, RFE
Dynamic Tests	Voltage Magnitude Step	System is balanced, at nominal frequency, without harmonics	Response Time, Delay Time, % Peak Overshoot
	Voltage Angle Step	System is balanced, at nominal frequency, without harmonics	Response Time, Delay Time, % Peak Overshoot
	Frequency Step	System is balanced, at nominal frequency, without harmonics	Frequency Response Time, ROCOF Response Time, Delay Time, % Peak Overshoot
	Frequency Ramp	System is balanced, at nominal frequency, without harmonics	FE, RFE
	Amplitude, Phase & Frequency Modulation	System is balanced, at nominal frequency, without harmonics	TVE, FE, RFE

The table 2.1 shows the library of test conditions used for analyzing the performance of PMUs. It can be seen from the table 2.1 that the PMU testing has been broadly classified as steady state tests and dynamic tests. The basic tests mentioned in the IEEE C37.118.1 Standard have been performed, in addition to which the tests have been performed under varying system conditions. It is important to test the PMU with parameter changes under different conditions, especially during the steady state performance analysis, as it is of utmost importance to analyze the behavior of the PMU under such realistic system conditions, for instance voltage and current magnitude changing when harmonics are present at off-nominal frequency conditions. The ranges of parameter or quantity variation (as mentioned in the 2nd column of table 2.1) and the thresholds of performance evaluation criteria (as mentioned in the 4th column of table 2.1) have been nearly kept the same as that mentioned in the standard. The change of system parameters (or quantities) has been scripted in RTDS Runtime as shown in fig. 2.3.

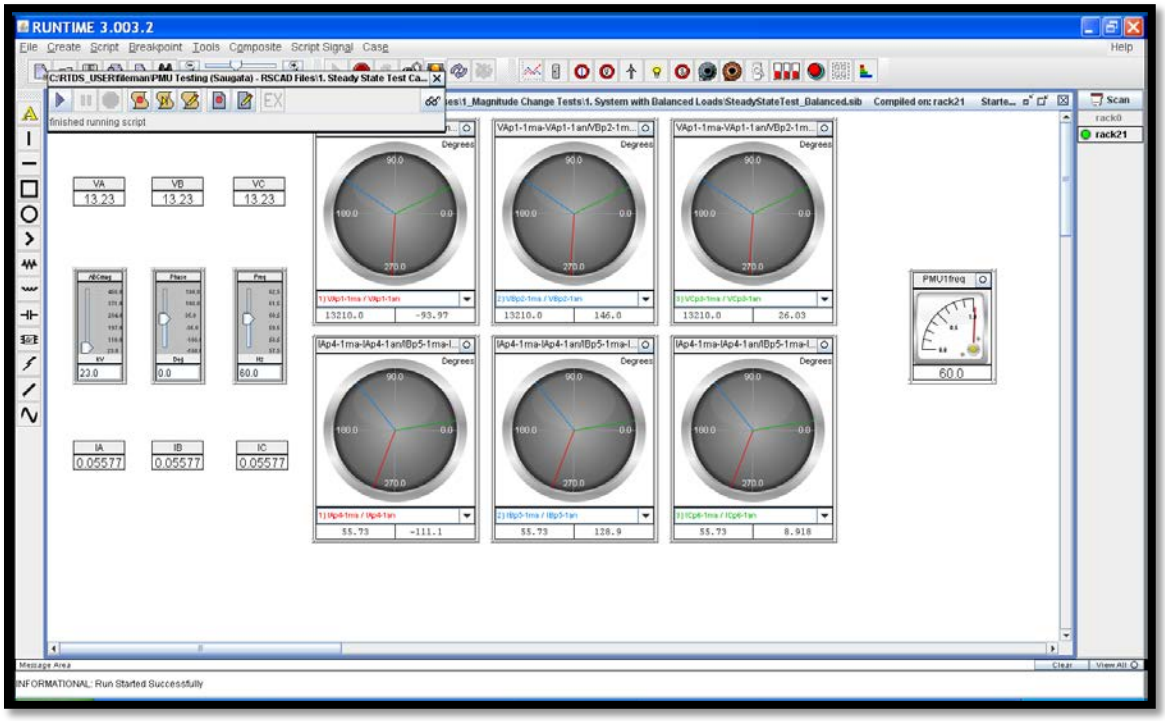

Figure 2.3: Example of RSCAD run case for obtaining test measurements

2.1.2.3 Performance of PMU Testing

Once the library of PMU test conditions is created in the RSCAD-RTDS, the PMU testing is performed in several stages. These include the following –

Step-1: Running the individual test cases in the RTDS

The RTDS draft case has the GTNET PMU connected in such a way that it gets the same input measurements as the test PMU. The test PMU gets the low level analog signals from the GTAO card of the RTDS. The GTAO card in turn gets the same input measurements as obtained by the GTNET PMU. With this configuration, individual script files have been written in the RTDS that keep changing the quantities and

parameters automatically as mentioned in table 2.1. These measurements obtained by running the test cases are fed into the GTNET PMU and the test PMU.

Step-2: Collecting the data of the individual test cases in the PDC from the PMUs
A PDC (SEL-5073) has been used to collect all the test data of steady state tests and dynamic tests from the PMU under test and the ideal PMU (i.e. the GTNET PMU in the RTDS) as shown in fig. 2.4. Following are the data that are archived in the PDC for the test PMUs and the GTNET PMU –

-> Time Stamp in the PMU
-> Voltage Magnitude of Phase A measured by the PMU
-> Voltage Angle of Phase A measured by the PMU
-> Voltage Magnitude of Phase B measured by the PMU
-> Voltage Angle of Phase B measured by the PMU
-> Voltage Magnitude of Phase C measured by the PMU
-> Voltage Angle of Phase C measured by the PMU
-> Current Magnitude of Phase A measured by the PMU
-> Current Angle of Phase A measured by the PMU
-> Current Magnitude of Phase B measured by the PMU
-> Current Angle of Phase B measured by the PMU
-> Current Magnitude of Phase C measured by the PMU
-> Current Angle of Phase C measured by the PMU
-> Frequency measured by the PMU
-> ROCOF measured by the PMU

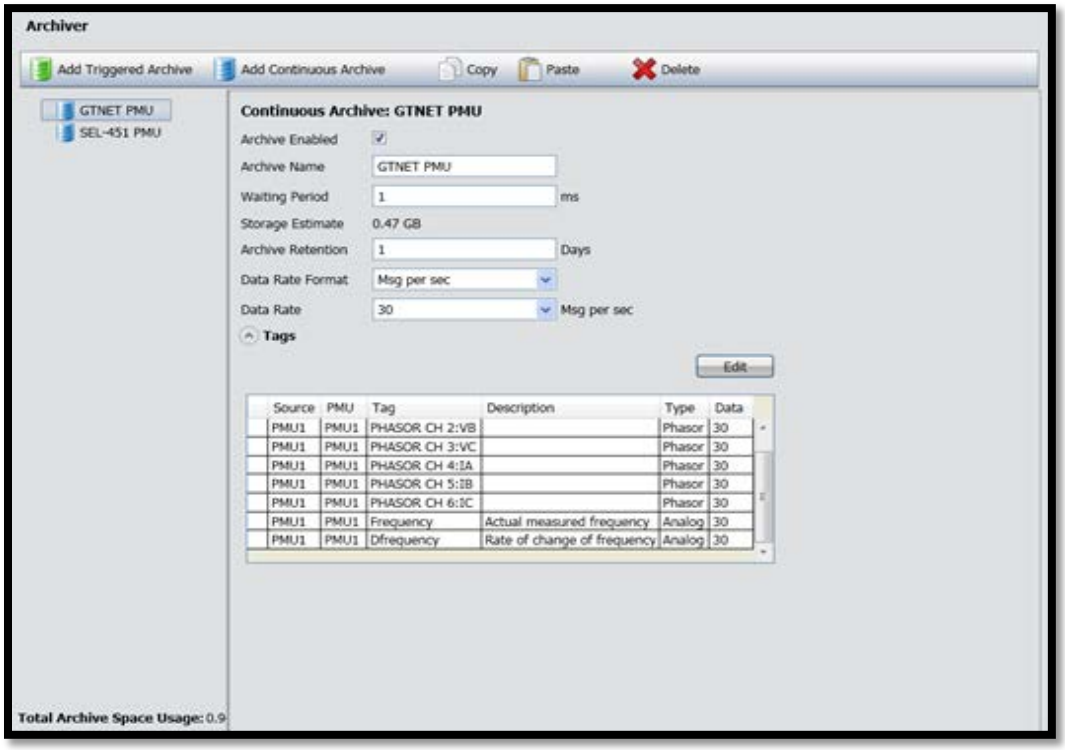

Figure 2.4: Example of data archival in software PDC

Step-3: Analysis of the data of the individual test cases based on IEEE-C37.118.1 Standard

Once all the data is archived in the PDC, this archived data is analyzed to find the conformance of the test PMU to the Standard requirements. The performance evaluation parameters for each test (as mentioned in table 2.1) are computed for the test data analysis as per the formulae mentioned in the Standard. Following is a brief description of these performance evaluation parameters -

(a) Total Vector Error (TVE) -

$$\mathrm{TVE}(n) = \sqrt{\frac{(\hat{X}_r(n) - X_r(n))^2 + (\hat{X}_i(n) - X_i(n))^2}{(X_r(n))^2 + (X_i(n))^2}}$$

Where, $\widehat{X_r}(n)$ and $\widehat{X_\iota}(n)$ are the sequences of estimates given by the test PMU, and *X*r(*n*) and *X*i(*n*) are the sequences of values of the measurements at the instants of time (*n*) read by the ideal PMU (GTNET PMU).

(b) Frequency Error (FE) -

$$\mathrm{FE} = = |f_{\mathrm{true}} - f_{\mathrm{measured}}|$$

Where, f_{true} is the frequency measured by the ideal PMU (GTNET PMU), and $f_{measured}$ is the frequency measured by the ideal PMU.

(c) Rate of Change of Frequency or ROCOF Error (RFE) -

$$\mathrm{RFE} = = |(\mathrm{d}f/\mathrm{d}t)_{\mathrm{true}} - (\mathrm{d}f/\mathrm{d}t)_{\mathrm{measured}}|$$

Where, $(\frac{df}{dt})_{true}$ is the ROCOF measured by the ideal PMU (GTNET PMU), and $(\frac{df}{dt})_{true}$ is the ROCOF measured by the test PMU.

(d) Measurement Response Time -

Measurement response time is the time to transition between two steady-state measurements before and after a step change is applied to the input. It shall be determined as the difference between the time that the measurement leaves a specified accuracy limit and the time it reenters and stays within that limit when a step change is applied to the PMU input. This shall be measured by applying a positive or negative step change in phase or magnitude or frequency to the PMU input signal. The input signal shall be held at a steady-state condition before and after the step change. The only input signal change during this test shall be the parameter that have been stepped.

(e) Measurement Delay Time -

Measurement delay time is defined as the time interval between the instant that a step change is applied to the input of a PMU and measurement time that the stepped parameter achieves a value that is halfway between the initial and final steady-state values. Both the step time and measurement time are measured on the UTC time scale. This measurement shall be determined by applying a positive or negative step change in phase or magnitude or frequency to the PMU input signal. The input signal shall be held

at a steady-state condition before and after the step change. The only input signal change during this test shall be the parameter(s) that have been stepped.

(f) Peak Overshoot -
This is the maximum value by which the measured value exceeds the final steady state value when a positive step change is applied in phase or magnitude or frequency to the PMU input signal. The input signal shall be held at a steady-state condition before and after the step change. The only input signal change during this test shall be the parameter(s) that have been stepped.

2.1.2.4 Conclusion from Test Results

All the tests mentioned in table 2.1 have been performed on PMUs from different vendors. The nature of PMU behavior are mostly the same qualitatively amongst those tested. In this section, the test conditions and results of 1 test PMU "PMU-A" have been discussed, which is a qualitative representation of the other PMUs that have been tested. Example of system test conditions in RSCAD is shown in fig. 2.5.

(A) Discussion on Steady State Tests -

→ Voltage & Current Magnitude Change during balanced system conditions:

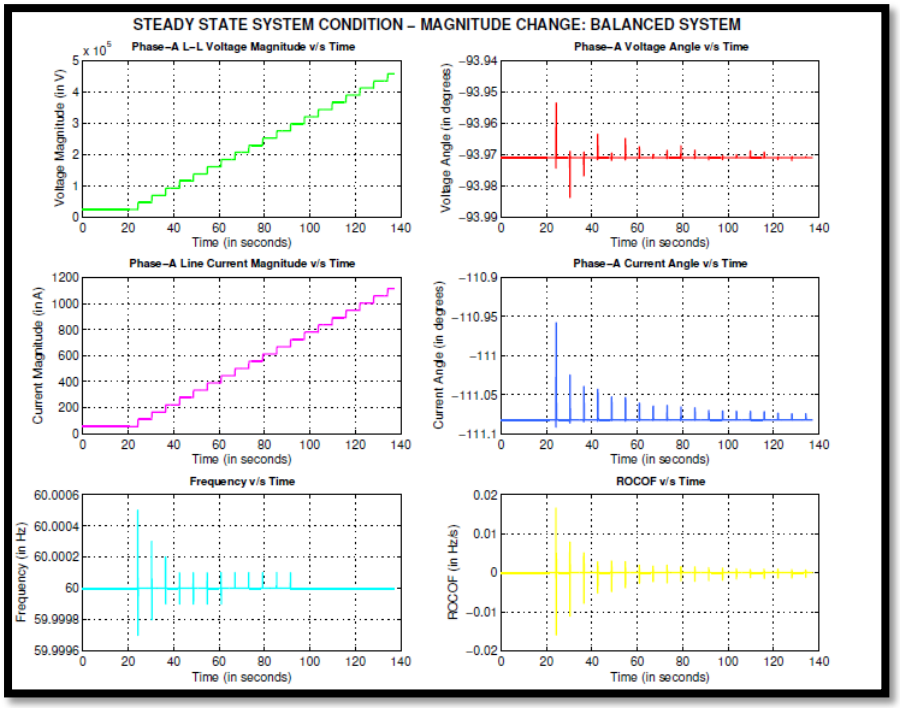

Figure 2.5: Test conditions for magnitude change (balanced, nominal)

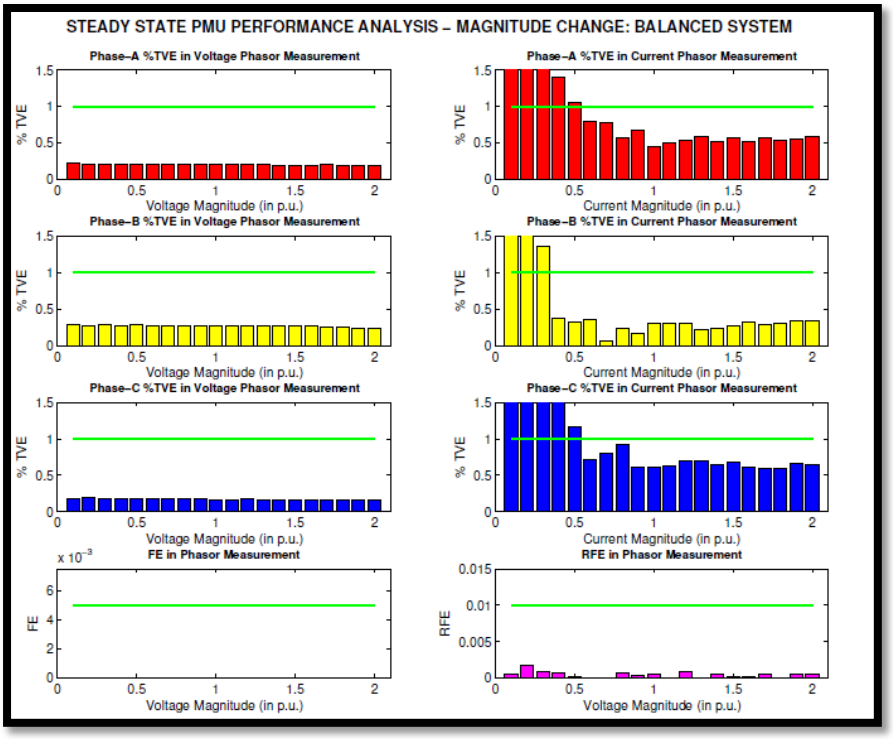

Figure 2.6: Error analysis for magnitude change (balanced, nominal)

From fig. 2.6, when the system is balanced and is at nominal frequency without harmonics, following observations can be made -

(i) The voltage TVEs of all the 3 phases are much lesser than the threshold value of 1%.
(ii) The voltage TVEs of all the 3 phases are not the same.
(iii) The current TVEs of all the 3 phases are very high (above 1%) when the PMU measures current phasors far below the nominal current value. Gradually, as the current measurement approaches the nominal value, the TVEs decrease and go below the permissible threshold of 1%.
(iv) The current TVEs of all the 3 phases are not the same.
(v) On the whole, current TVEs are found to be significantly higher than the voltage TVEs.
(vi) FE is much below the permissible threshold value.
(vii) RFE is also much below the allowed threshold value.

→ Voltage & Current Magnitude Change under Off-nominal system frequency conditions:

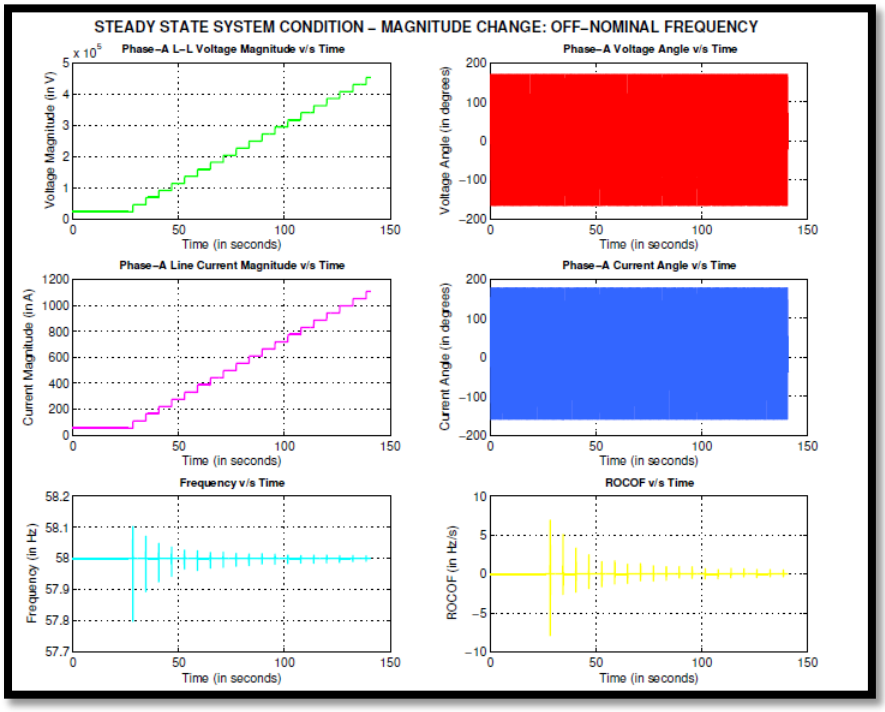

Figure 2.7: Test conditions for magnitude change (balanced, off-nominal)

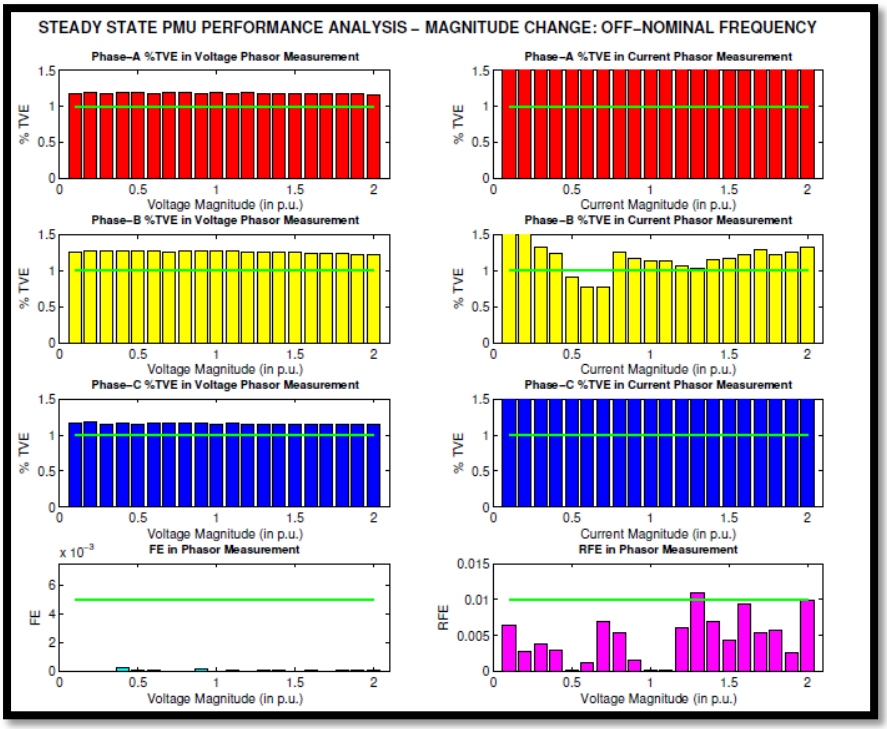

Figure 2.8: Error analysis for magnitude change (balanced, off-nominal)

Fig. 2.7 shows system test condition in RTDS. As shown in fig. 2.8, when the system is balanced and is at off-nominal frequency (58 Hz) without harmonics, following observations can be made -

(i) The voltage TVEs of all the 3 phases are higher than the threshold value of 1%.
(ii) The voltage TVEs of all the 3 phases are not the same.
(iii) The current TVEs of all the 3 phases are very much higher than the allowed threshold of 1%.
(iv) The current TVEs of all the 3 phases are not the same.
(v) On the whole, current TVEs are found to be significantly higher than the voltage TVEs.
(vi) FE is much below the permissible threshold value, but is a little higher than the test condition when the system frequency was at nominal value.
(vii) RFE is higher than the test case when the system frequency was at nominal value. It can be seen that at some point, the RFE also has exceeded the allowed threshold value.

→ Voltage & Current Magnitude Change under when harmonics (3rd, 5th, 7th, and 9th orders) exist in the system:

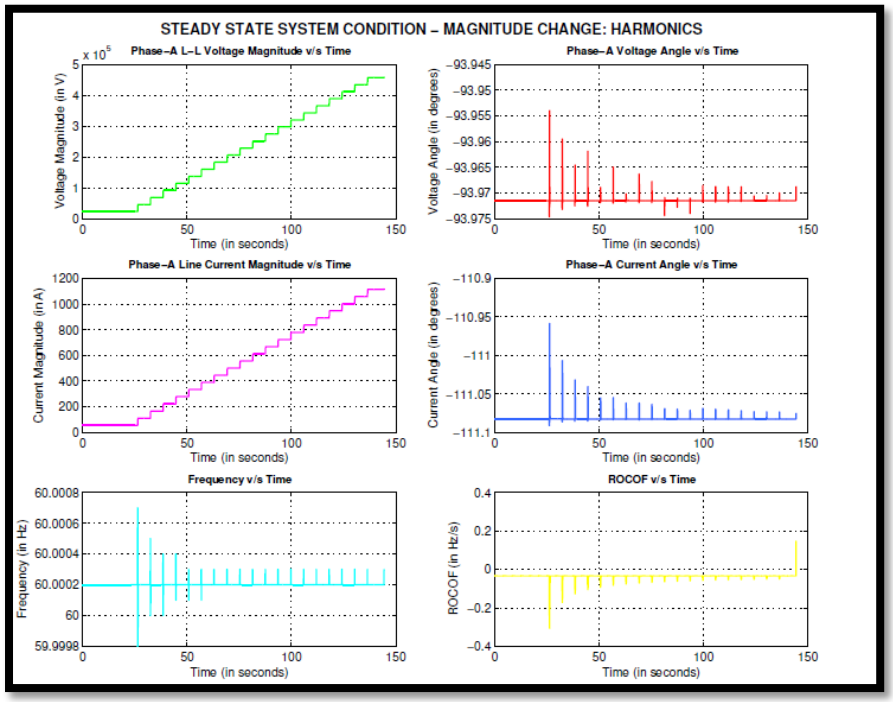

Figure 2.9: Test conditions for magnitude change (harmonics, nominal)

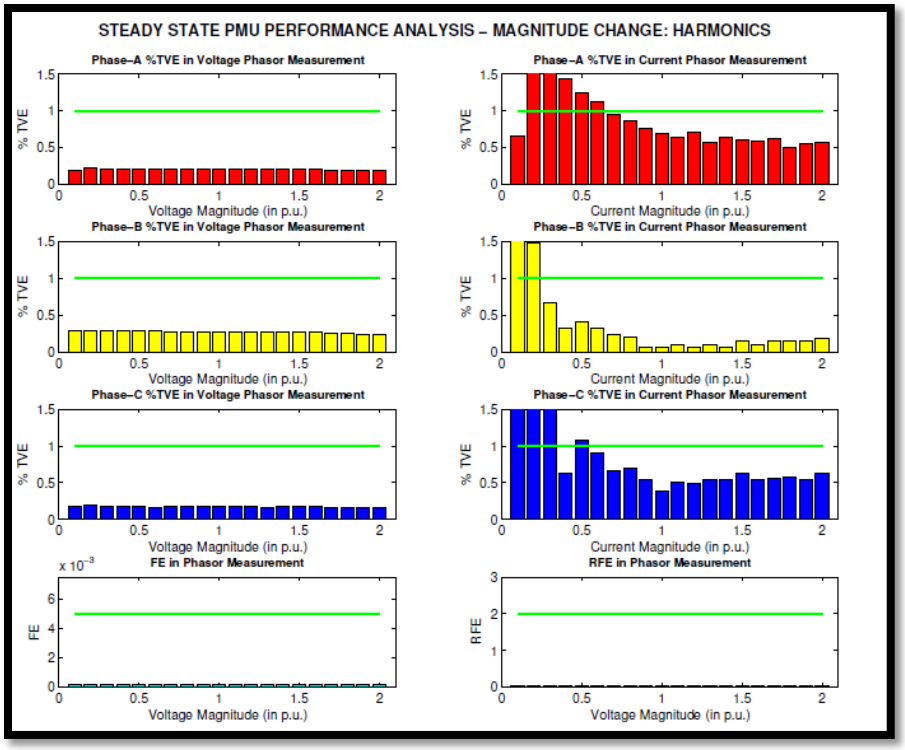

Figure 2.10: Error analysis for magnitude change (harmonics, nominal)

Fig. 2.9 shows the test conditions and fig. 2.10 shows error analysis. When the system is balanced and is at nominal frequency with harmonics, following observations can be made-

(i) The voltage TVEs of all the 3 phases are much lesser than the threshold value of 1%.
(ii) The voltage TVEs of all the 3 phases are not the same.
(iii) The current TVEs of all the 3 phases are very high (above 1%) when the PMU measures current phasors far below the nominal current value. Gradually, as the current measurement approaches the nominal value, the TVEs decrease and go below the permissible threshold of 1%.
(iv) The current TVEs of all the 3 phases are not the same.
(v) On the whole, current TVEs are found to be significantly higher than the voltage TVEs.
(vi) FE is much below the permissible threshold value. If a comparison is made with the test cases when harmonics are not present, it has been seen that the average FE is much higher when harmonics are present. This is an expected behavior, because of which the IEEE Standard has also increased the permissible threshold value of FE when harmonics are present.
(vii) RFE is also much below the allowed threshold value. If a comparison is made with the test cases when harmonics are not present, it has been seen that the average RFE is much higher when harmonics are present. This is also an expected behavior, because of which the IEEE Standard has also increased the permissible threshold value of RFE when harmonics are present.

→ Voltage & Current Magnitude Change under Off-nominal system frequency conditions when harmonics are also present:

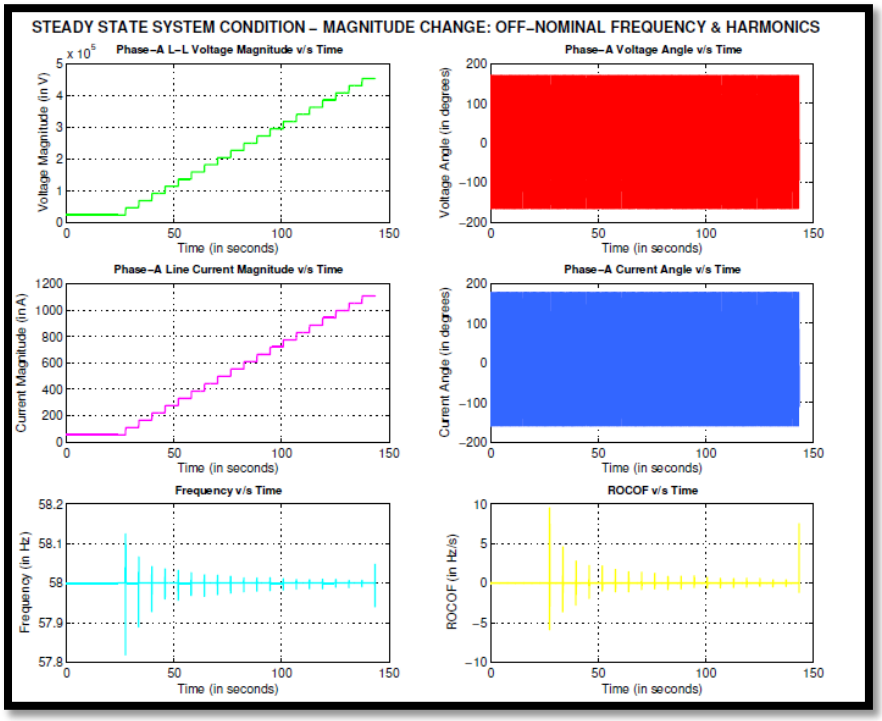

Figure 2.11: Test conditions for magnitude change (harmonics, off-nominal)

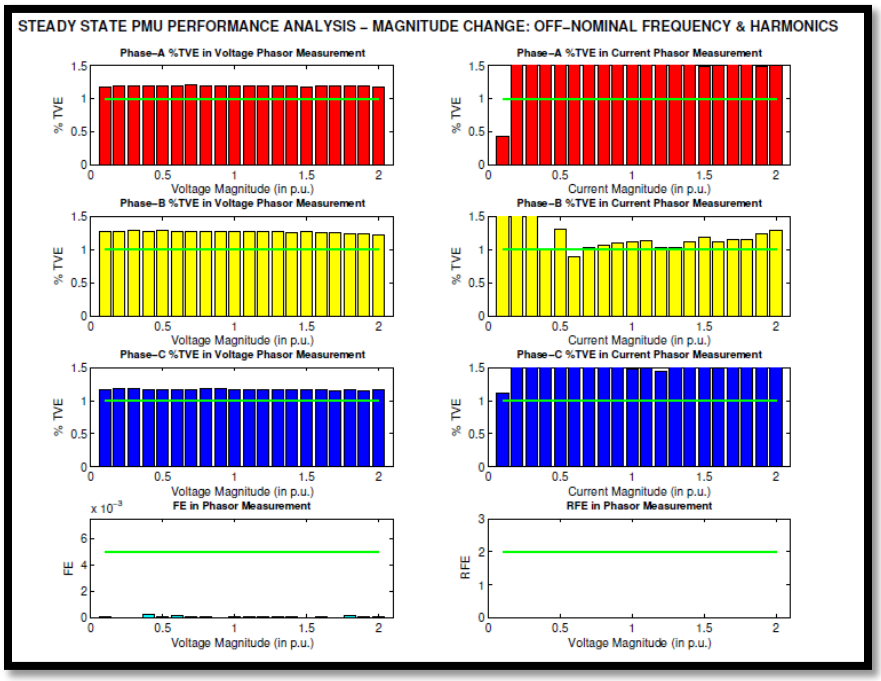

Figure 2.12: Error analysis for magnitude change (harmonics, off-nominal)

Based on test condition of fig. 2.11, and fig. 2.12, when the system is balanced and is at off-nominal frequency with harmonics, following observations can be made -

(i) The voltage TVEs of all the 3 phases are higher than the threshold value of 1%.
(ii) The voltage TVEs of all the 3 phases are not the same.
(iii) The current TVEs of all the 3 phases are very much higher than the allowed threshold of 1%.
(iv) The current TVEs of all the 3 phases are not the same.
(v) On the whole, current TVEs are found to be significantly higher than the voltage TVEs.
(vi) FE is much below the permissible threshold value. If a comparison is made with the test cases when harmonics are not present, it has been seen that the average FE is much higher when harmonics are present. This is an expected behavior, because of which the IEEE Standard has also increased the permissible threshold value of FE when harmonics are present.
(vii) RFE is also much below the allowed threshold value. If a comparison is made with the test cases when harmonics are not present, it has been seen that the average RFE is much higher when harmonics are present. This is also an expected behavior, because of which the IEEE Standard has also increased the permissible threshold value of RFE when harmonics are present.
(viii) Amongst all the test conditions discussed above when the voltage and current magnitudes are changed, the performance of the PMU deteriorates the most when the system is at off-nominal frequency and also has harmonics.

→ Voltage & Current Angle Change under balanced system conditions:

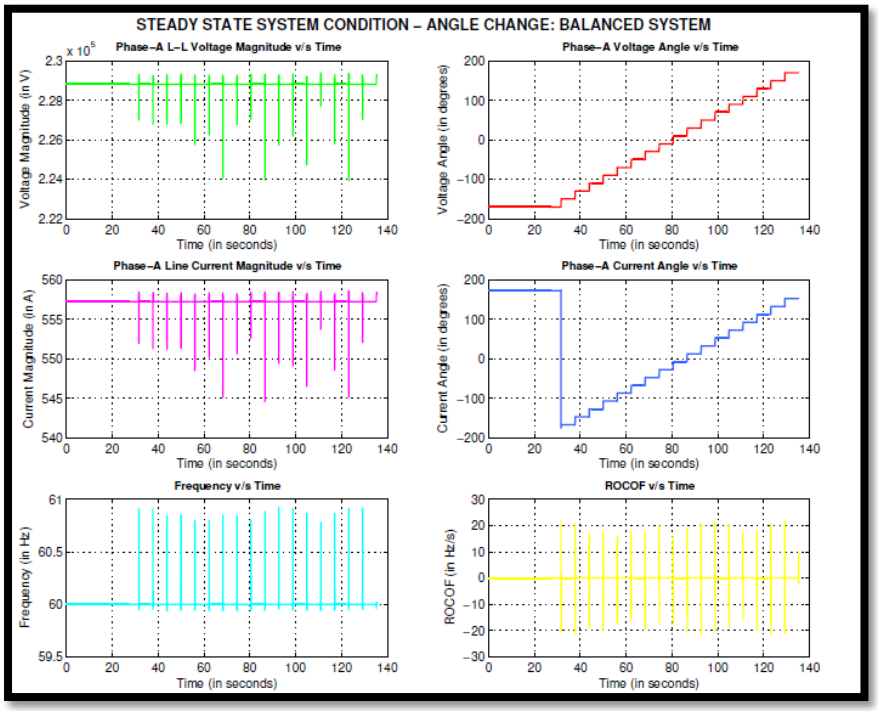

Figure 2.13: Test conditions for angle change (balanced, nominal)

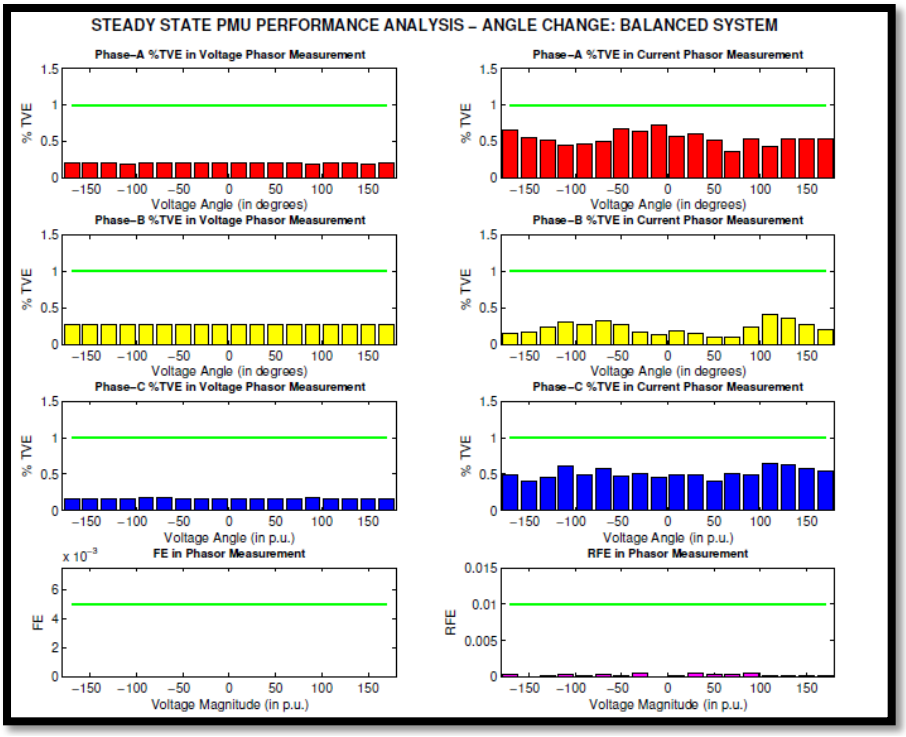

Figure 2.14: Error analysis for angle change (balanced, nominal)

From fig. 2.13 and fig. 2.14, when the system is balanced and is at nominal frequency without harmonics, following observations can be made –

(i) The voltage TVEs of all the 3 phases are much lesser than the threshold value of 1%.
(ii) The voltage TVEs of all the 3 phases are not the same.
(iii) The current TVEs of all the 3 phases are lesser than the permissible threshold of 1%.
(iv) The current TVEs of all the 3 phases are not the same.
(v) On the whole, current TVEs are found to be higher than the voltage TVEs.
(vi) FE is much below the permissible threshold value.
(vii) RFE is also much below the allowed threshold value.

→ Voltage & Current Angle Change under when harmonics (3rd, 5th, 7th, and 9th orders) exist in the system:

From fig. 2.15 and 2.16 when the system is balanced and is at nominal frequency with harmonics, following observations can be made –

(i) The voltage TVEs of all the 3 phases are much lesser than the threshold value of 1%.
(ii) The voltage TVEs of all the 3 phases are not the same.
(iii) The current TVEs of all the 3 phases are very high (above 1%) irrespective of the current magnitude.
(iv) The current TVEs of all the 3 phases are not the same.

(v) On the whole, current TVEs are found to be significantly higher than the voltage TVEs.

(vi) FE is much below the permissible threshold value. If a comparison is made with the test cases when harmonics are not present, it has been seen that the average FE is much higher when harmonics are present. This is an expected behavior, because of which the IEEE Standard has also increased the permissible threshold value of FE when harmonics are present.

(vii) RFE is also below the allowed threshold value. If a comparison is made with the test cases when harmonics are not present, it has been seen that the average RFE is much higher when harmonics are present. This is also an expected behavior, because of which the IEEE Standard has also increased the permissible threshold value of RFE when harmonics are present.

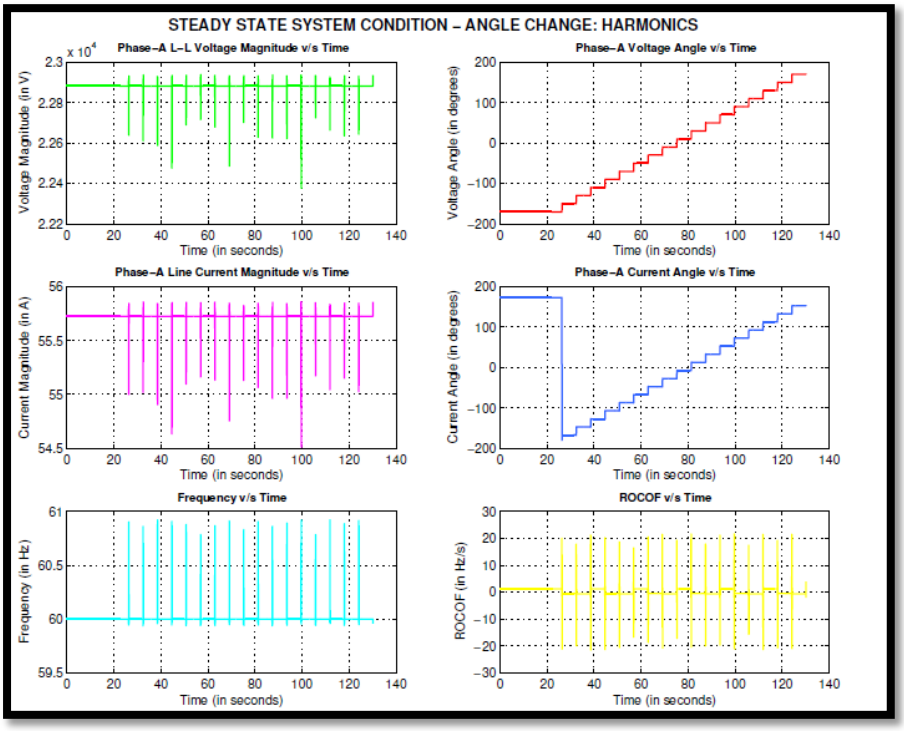

Figure 2.15: Test conditions for angle change (harmonics, nominal)

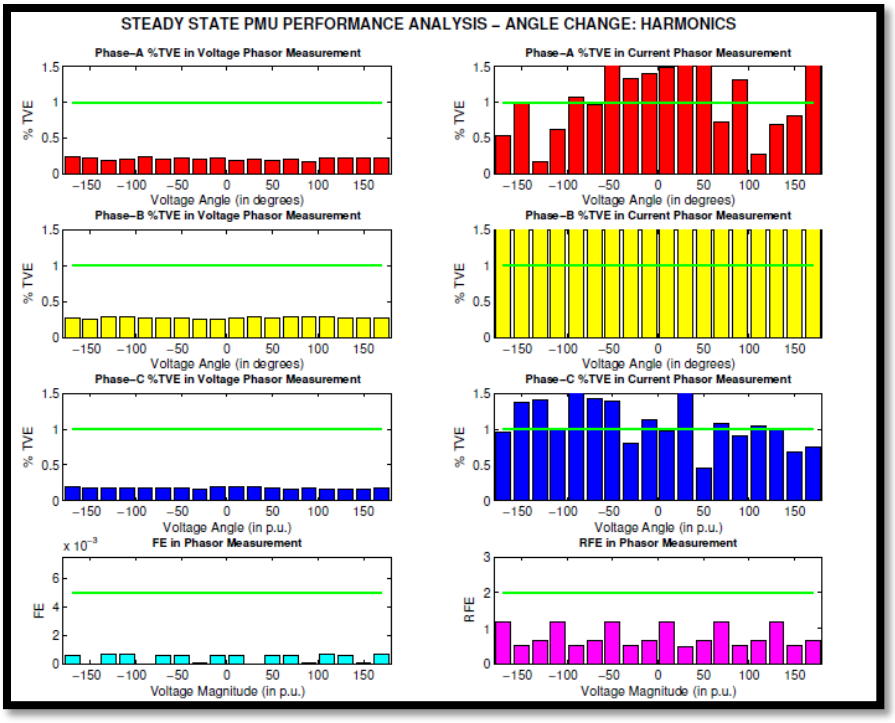

Figure 2.16: Error analysis for angle change (harmonics, nominal)

→ Frequency Change under balanced system conditions:

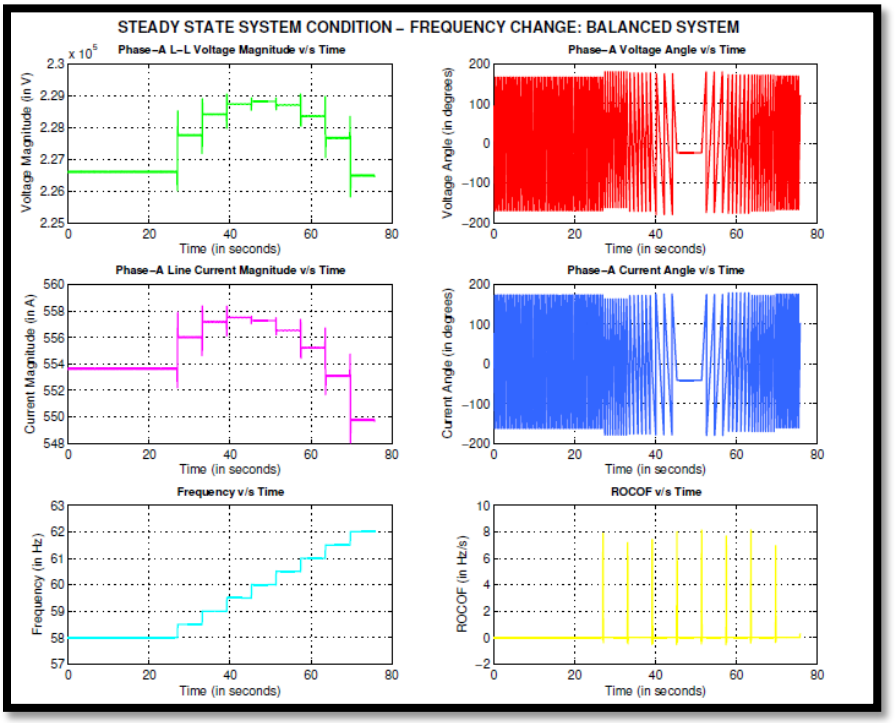

Figure 2.17: Test conditions for frequency change (balanced)

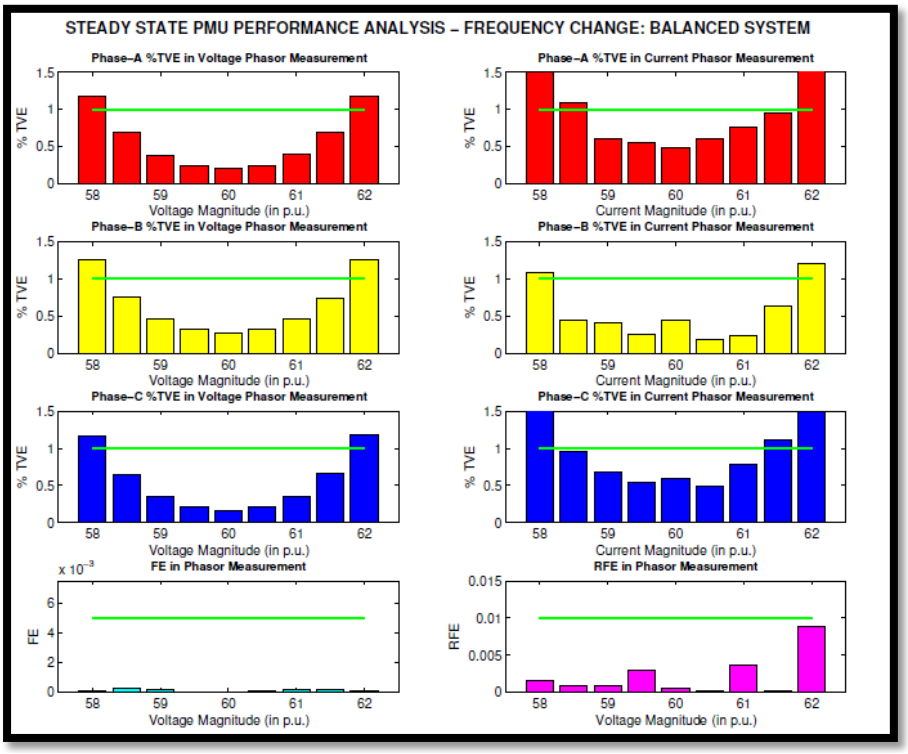

Figure 2.18: Error analysis for frequency change (balanced)

Based on test conditions in fig. 2.17 and error analysis from fig. 2.18, when the system is balanced without harmonics, following observations can be made -

(i) The voltage TVEs of all the 3 phases are much lesser than the threshold value of 1% when the system is at nominal frequency (60 Hz). However, as the system frequency moves away from the nominal value both, above and below, the TVEs start increasing rapidly. It can be seen that at 58 Hz and 62 Hz, the voltage TVEs exceed the threshold value of 1%.

(ii) The voltage TVEs of all the 3 phases are not the same.

(iii) The current TVEs of all the 3 phases are lesser than the threshold value of 1% when the system is at nominal frequency (60 Hz). However, as the system frequency moves away from the nominal value both, above and below, the TVEs start increasing rapidly. It can be seen that at 58 Hz and 62 Hz, the current TVEs exceed the threshold value of 1%.

(iv) The current TVEs of all the 3 phases are not the same.

(v) On the whole, current TVEs are found to be higher than the voltage TVEs.

(vi) FE is much below the permissible threshold value.

(vii) RFE is also below the allowed threshold value.

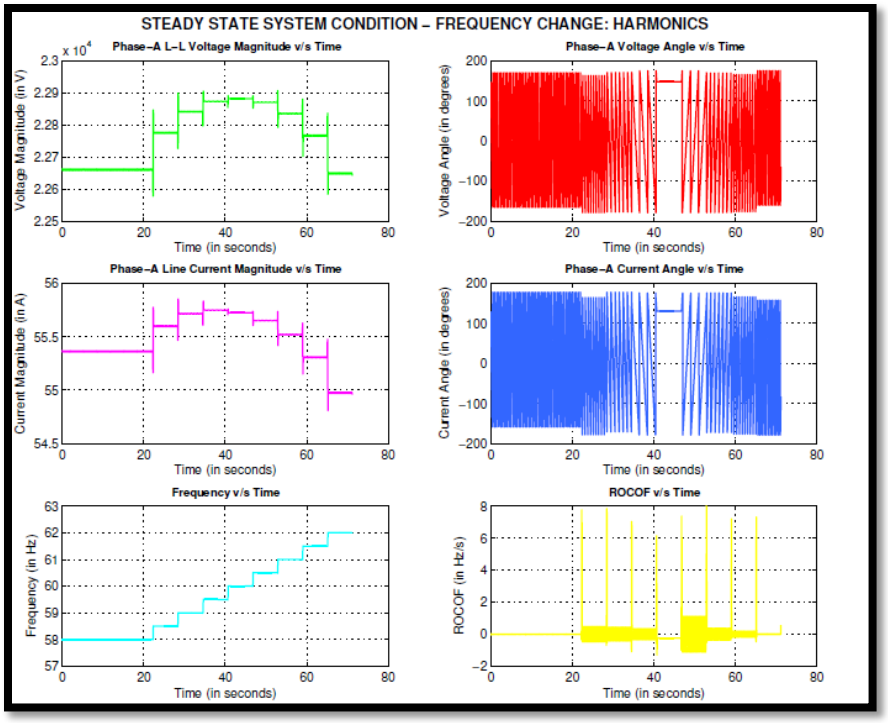

Figure 2.19: Test conditions for frequency change (balanced, harmonics)

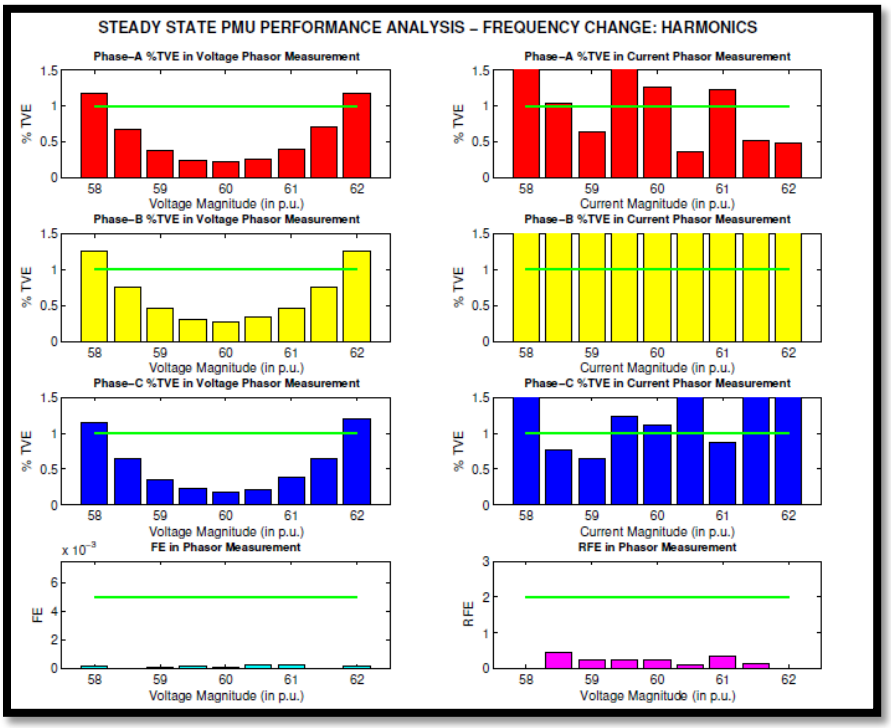

Figure 2.20: Error analysis for frequency change (balanced, harmonics)

From fig. 2.19 and fig. 2.20, when the system is balanced with harmonics, following observations can be made -

(i) The voltage TVEs of all the 3 phases are much lesser than the threshold value of 1% when the system is at nominal frequency (60 Hz). However, as the system frequency moves away from the nominal value both, above and below, the TVEs start increasing rapidly. It can be seen that at 58 Hz and 62 Hz, the voltage TVEs exceed the threshold value of 1%.
(ii) The voltage TVEs of all the 3 phases are not the same.
(iii) The current TVEs of all the 3 phases are mostly higher than the threshold value of 1% and are quite random independent of the frequency values unlike voltage TVEs.
(iv) The current TVEs of all the 3 phases are not the same.
(v) On the whole, current TVEs are found to be higher than the voltage TVEs.
(vi) FE is much below the permissible threshold value.
(vii) RFE is also below the allowed threshold value.

(B) Discussion on Dynamic Tests -

→ Voltage Magnitude Step Change:

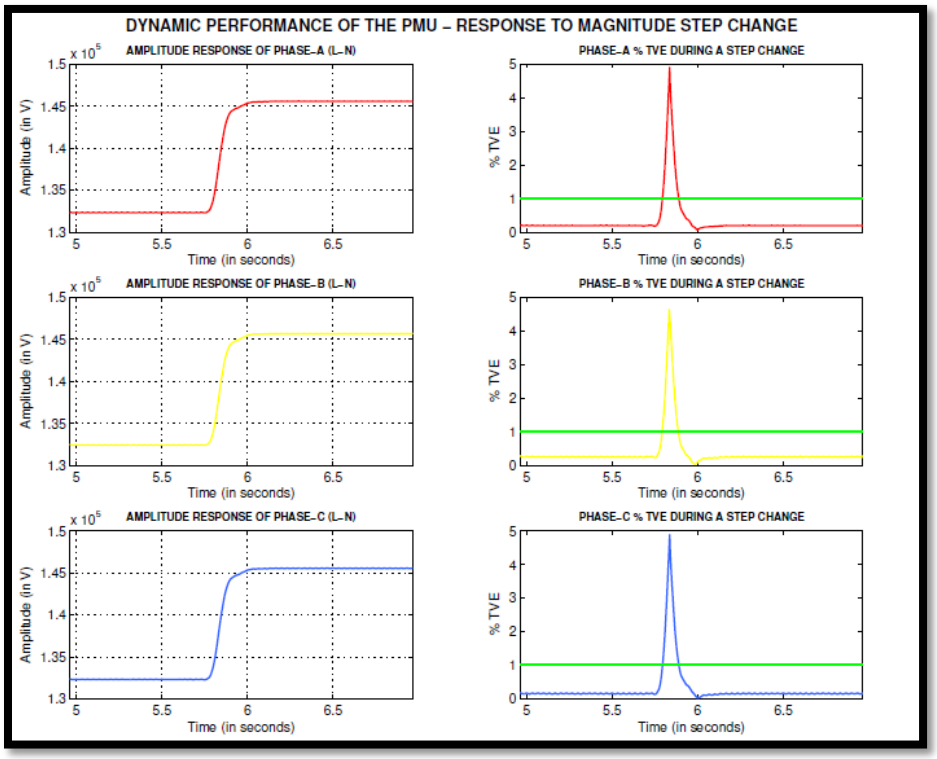

Figure 2.21: Response during step change in voltage magnitude

Following are the analytical results of the PMU performance during the step change in voltage magnitude (fig. 2.21) -

Table 2.2: Test results for response to magnitude step change

Evaluation Parameters	Results of the Test PMU	Allowable Values as per IEEE-C37.118.1
Response Time (in seconds)	0.093	0.182
Delay Time (in seconds)	0.065	0.008
% Peak Overshoot	0.279	10

From the results table 2.2, it can be seen that the PMU under test -

(i) Meets the requirement of response time.

(ii) Does not meet the requirement of delay time

(iii) Meets the requirement of % peak overshoot

→ Voltage Angle Step Change:

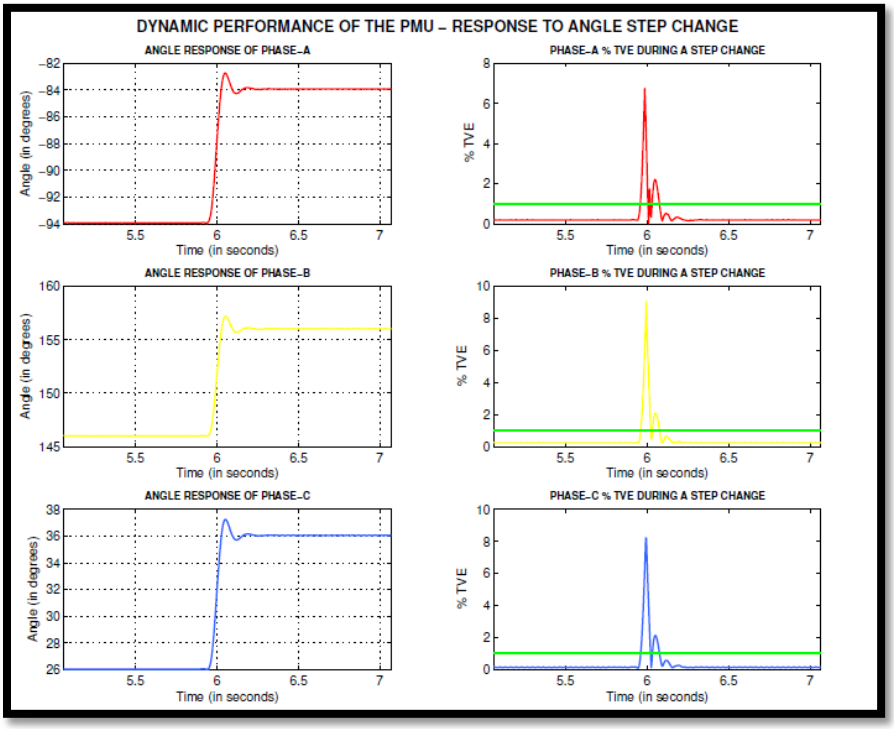

Figure 2.22: Response during step change in voltage angle

Table 2.3: Test results for response to angle step change

Evaluation Parameters	Results of the Test PMU	Allowable Values as per IEEE-C37.118.1
Response Time (in seconds)	0.113	0.182
Delay Time (in seconds)	0.045	0.008
% Peak Overshoot	2.561	10

From the results as shown in fig. 2.22 and table 2.3, it can be seen that the PMU under test-

(i) Meets the requirement of response time.
(ii) Does not meet the requirement of delay time
(iii) Meets the requirement of % peak overshoot

→ Frequency Step Change:

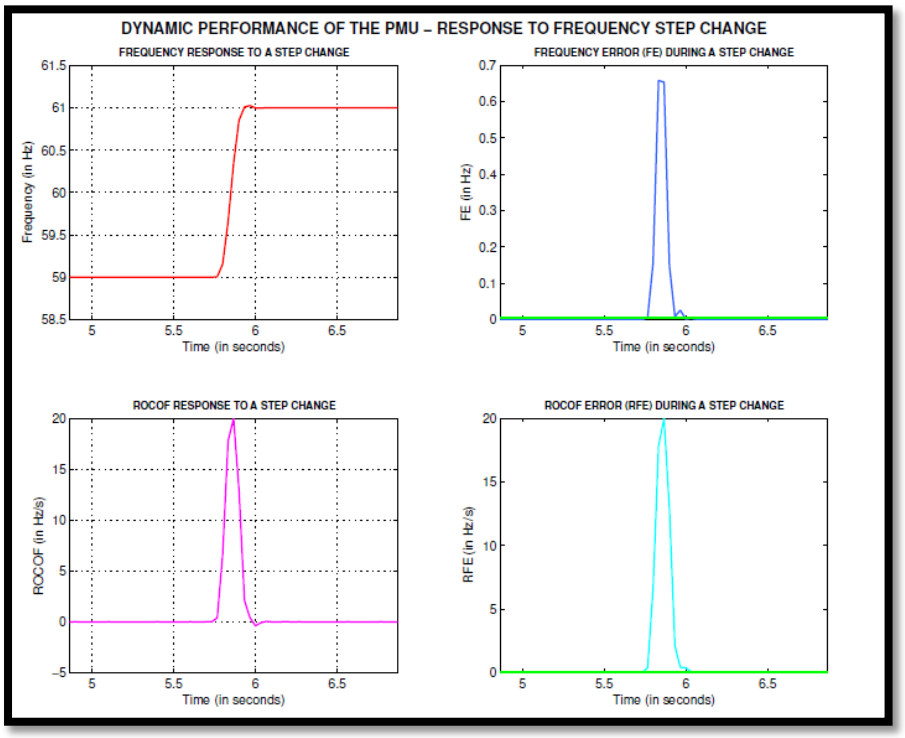

Figure 2.23: Response during step change in frequency

Table 2.4: Test results for response to frequency step change

Evaluation Parameters	Results of the Test PMU	Allowable Values as per IEEE-C37.118.1
Response Time (in seconds)	0.267	0.305
ROCOF Response Time (in seconds)	0.4	0.314
Delay Time (in seconds)	0.08	0.008
% Peak Overshoot	0.042	10

From the results shown in fig. 2.23 and table 2.4, it can be seen that the PMU under test -

(i) Meets the requirement of frequency response time
(ii) Does not meet the requirement of ROCOF response time
(iii) Does not meet the requirement of delay time
(iv) Meets the requirement of % peak overshoot

→ Frequency Ramp Change:

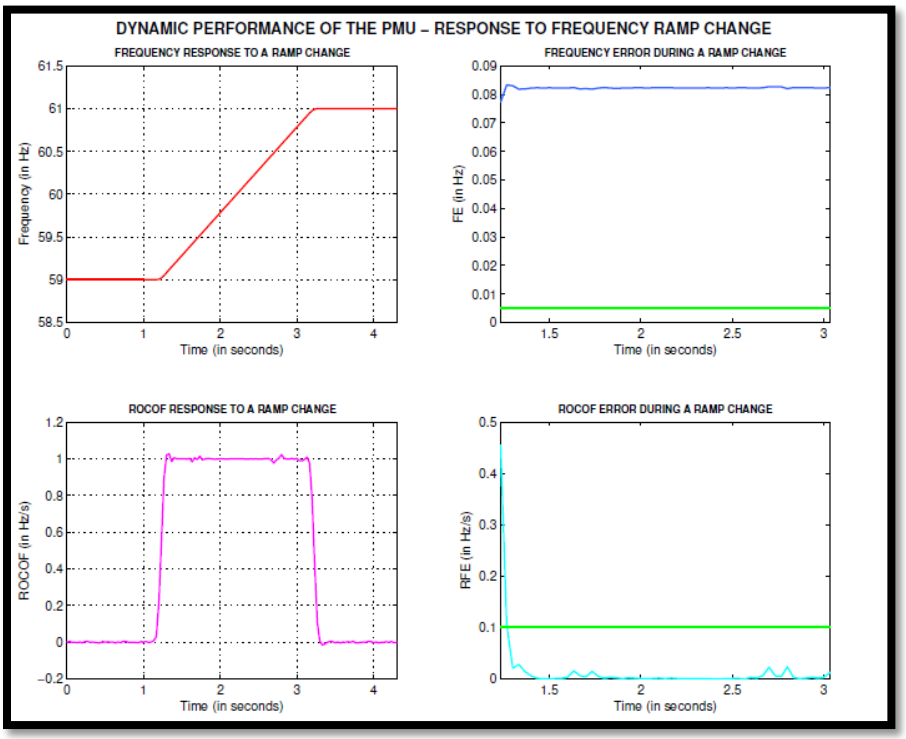

Figure 2.24: Response during ramp change in frequency

Table 2.5: Test results for response to frequency ramp change

Evaluation Parameters	Results of the Test PMU	Allowable Values as per IEEE-C37.118.1
Maximum FE (in Hz)	0.083	0.005
Maximum RFE (in Hz/s)	0.457	0.1

From the results as shown in fig. 2.24 and table 2.5, it can be seen that the PMU under test-

(i) Does not meet the requirement of FE
(ii) Does not meet the requirement of RFE

→ Amplitude, Phase & Frequency Modulation Changes:
From fig. 2.25 and 2.26, when the amplitude, phase and frequency modulation is done in the system, following observations can be made -

(i) The voltage TVEs of all the 3 phases are much higher than the threshold value of 1%.
(ii) The voltage TVEs of all the 3 phases are not the same.
(iii) The current TVEs of all the 3 phases are much higher than the threshold value of 1%.
(iv) The current TVEs of all the 3 phases are not the same.

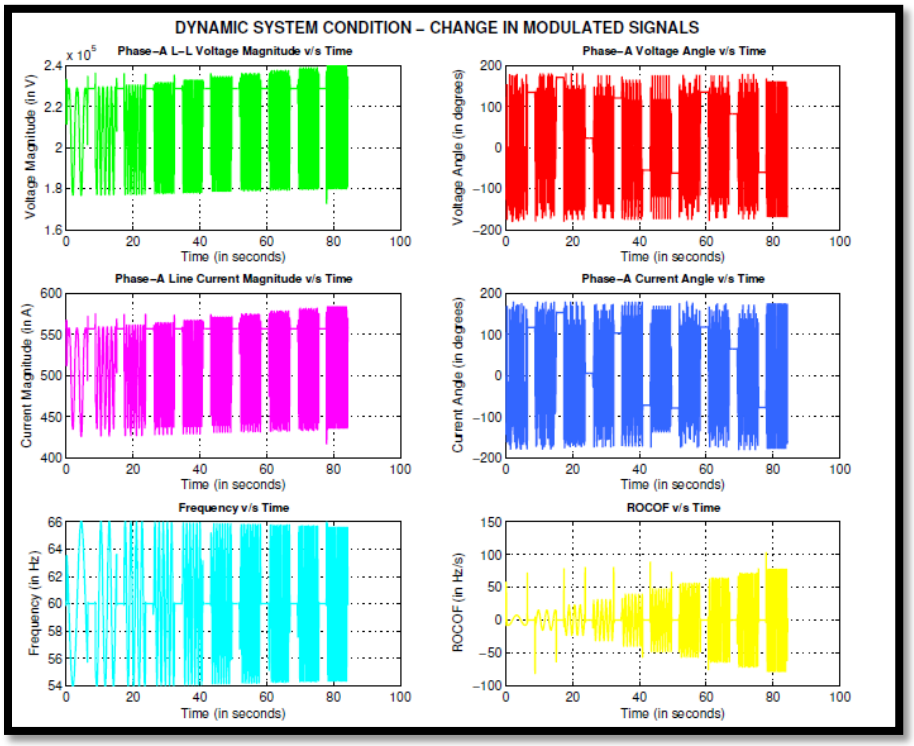

Figure 2.25: Dynamic test conditions for change in modulated signal

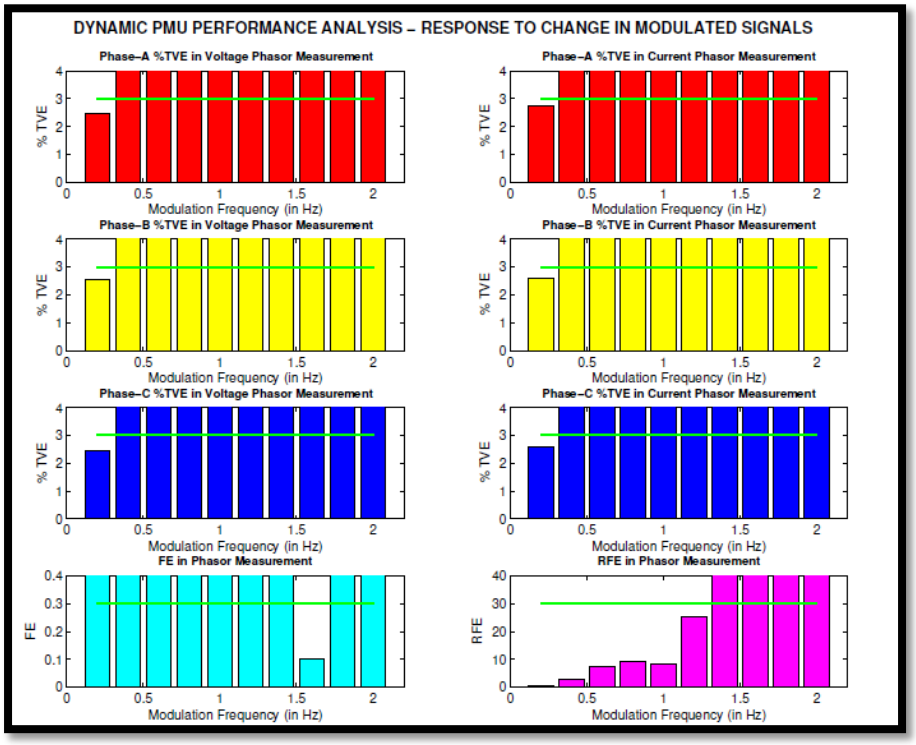

Figure 2.26: Error analysis of the test PMU under given system condition

(v) On the whole, current TVEs are found to be higher than the voltage TVEs.
(vi) FE is much higher than the permissible threshold value.
(vii) RFE is initially below the allowed threshold limit. But as the frequency modulation increases, the RFE goes on increasing rapidly, and exceeds the allowed threshold value.

From the analysis of the steady state and dynamic tests, it can be seen that the PMU under test behaves differently under different system conditions. The tests performed on the PMU under test provides a comprehensive coverage of the performance of the PMU. It has been seen that the PMU under test satisfies most of the test criteria as mentioned in the standard, but fails some of them.

2.2.3 PDC Testing

2.1.3.1 Introduction

A Phasor Data Concentrator (PDC) works as a node in a communication network where synchrophasor data from a number of PMUs or PDCs is processed and fed out as a single stream to the higher level PDCs and/or applications. Synchrophasor data may include time stamped 3-phase voltage magnitudes, voltage angles, current magnitudes, current angles, frequency, rate of change of frequency (ROCOF), real and reactive power, digital signals like circuit breaker switch status, etc. The PDC processes synchrophasor data by timestamp to create a system-wide measurement set.

PDCs can have several modes of operation. For instance, the local PDCs aggregate and time-align synchrophasor data from multiple PMUs in a substation and feed the data to applications. Mid-level and higher-level PDCs collect synchrophasor data from multiple PDCs, conduct data quality checks, time align the data and feed the data to applications. The PDCs may be recognized as a function rather than as a stand-alone device or hardware/software package, and can be integrated into other systems and devices. A structured hierarchy of distributed PDCs may be formed to serve a hierarchy of systems: substation, utility, control area, reliability coordinator, and interconnection level. Distributed PDCs may also interact with each other on a peer-to-peer basis among utilities, control areas, and reliability coordinators.

A PDC is expected to perform some of the important functions in the synchrophasor infrastructure as stated below -

(a) Data Aggregation -
This is the basic function of a PDC. It refers to the streaming and accumulation of the synchrophasor data from the PMU(s) in the PDC. The data aggregation functionality of a PDC is required for real time system monitoring as well as post-event analysis. Data aggregation function could be performed with or without time alignment. It should preserve data quality, time quality, and time synchronization indications from each signal, and include the data quality information assigned by the individual sending devices to the output data frames.

Data coming into a PDC has been time stamped by the PMU with a time referenced to UTC, absolute time. Data aggregation with time alignment refers to waiting for data with a given timestamp from all sources, placing that data in a packet, and forwarding it. The PDC aligns the data received from PMU/PDC according to their timestamps, not their arriving order or arriving time. Time alignment to absolute time refers to waiting no more than a specified absolute wait time after a timestamp time for data with that timestamp. This requires that the PDC is synchronized to UTC. Time alignment to relative time refers to waiting no more than a specified relative wait time after an event. An event may be the arrival of the first data with a specific timestamp.

For some applications, it is desirable to receive a set of synchrophasor measurements with minimum latency. However, to reduce data loss due to late data arrival, longer wait times are needed, which in turn increase latency. To address these conflicting requirements i.e. no loss of data due to late arrival and minimum latency, a PDC could aggregate all the data required for the output destination without time alignment and transmit it periodically.

(b) Data Forwarding -
To minimize PDC latency, a PDC needs to support data forwarding. Data forwarding is performed either from one input to one output, or from one input to multiple outputs. No data aggregation is performed in this case. Data forwarding can be performed without data modification or with data modifications that may include data format and coordinate conversion, phase and magnitude adjustments (for calibration purposes), decimation, interpolation, etc.

(c) Data Validation -
A PDC is supposed to perform basic data validation and check the data arriving at the PDC. This includes checking the time quality of all PMUs as well as the data status flags. For this purpose, data integrity checks such as cyclic redundancy check [CRC] can be performed on all received data. Any errors detected and suspected corrupt data should be flagged in output data stream(s).

(d) Data Communication -
This function allows a PDC to connect with other devices via serial and Ethernet based communication networks so that the PDC can receive synchrophasor data. The synchrophasor system communications include both data (streaming data and configuration information) and command communications. Data transfer is typically client-server based using either auto-initiation or a data request command. In the auto-initiation mode, data transmission is implemented without waiting for any request from any destination devices/applications for each individual data point in the series. In the data request command mode of operation a client (the PDC) sends a data request command to the server (a PMU or another PDC). The server then responds with the requested data. The data communications in a synchrophasor system could be one-to-one (i.e., from one source to one destination) and/or one-to-many (i.e., from one source to multiple destinations). Either mode may be implemented on Ethernet based networks, but serial networks are generally one-to-one unless the serial connection is specially modified

to allow a one-to-many connection. The command communications of a synchrophasor system includes various synchrophasor command frames. For example for IEEE Std C37.118.2-2011, the synchrophasor command frames provide commands to the PMU to initiate streaming, to stop streaming, to retrieve the header frame, to retrieve the configuration frame, and to execute user-defined controls. The command communications of a synchrophasor system may be one-to-one using serial or Ethernet networks. When using Ethernet networks, command communications typically uses TCP over IP, but can also use UDP over IP. Command communications are independent of the protocols used for the data transmission.

(e) Data Transfer Protocols Support and Conversion -
Synchrophasor data from PMUs may be available in different synchrophasor data transfer protocols such as IEEE Standard C37.118, IEEE Standard 1344-1995, IEC 61850-90-5, etc. A PDC should be able to support at least one of these protocols for seamless streaming of data from the PMU(s) it is connected to. If a PDC supports multiple synchrophasor data transfer protocols, it should convert synchrophasor data from one synchrophasor data transfer protocol to another to the extent possible.

(f) Data Latency Computation -
In a packet-switched network, data latency is the time delay between a sender transmitting a packet and a user receiving it. Because communication traffic volume and errors in transmission can affect intermediate delays, latency is sometimes not very predictable. Applied to the PMU/PDC system, there are multiple sources of synchrophasor data latency could be due to the following reasons -

(i) Physical distance between the two ends of the system,
(ii) Processing of the packet in intermediate network devices,
(iii) PMU calculation and processing time,
(iv) PMU–PDC data transmission time,
(v) PDC processing time.

Data latency will be different at different points in a hierarchical data network. It will increase cumulatively at successive data destinations such as the substation PDC, the TO control center PDC, the ISO control center PDC.

(g) Reporting Rate Conversion -
The reporting rate conversion refers to the change of the reporting rate of a data stream to be different from the input data stream (e.g., 30 frames per second (fps) to 15 fps, or 30 fps to 60 fps). Reporting rate conversion functions are very useful for -

(i) Merging synchrophasor data arriving at different reporting rates from different sources,
(ii) Converting available data to a rate that is most suitable for a specific application using synchrophasor data.

A PDC should ideally include both down-conversion and up-conversion functions. If this function is not provided, it should be clearly stated in the PDC's specification by the manufacturer. Along with this, any limitations in the conversion functions should also be specified. The PDC should support input rate conversion from all rates specified in IEEE

Standard C37.118.1-2011 to output streams having any rate specified in IEEE Std C37.118.1-2011. Reporting rate conversion should be user-configurable to accommodate the compatibility needs of all the devices and applications in the synchrophasor system, as well as all the applications that might be using the data from the PDC.

(h) Data Adjustments -
The PDC function requires the incoming data to be either copied into the output data stream, or converted to a different format (e.g., rectangular/polar, floating/fixed point). The data are expected to be essentially unchanged. However, at times, a PDC may be required to perform magnitude or phase adjustments on the incoming signal. There could be two types of such adjustments:

(i) Calibration type adjustments,
(ii) Bulk type adjustments.

Each of these adjustments is expected to be set manually, based on calibration factors, phase rotation sequence, transformer ratios, phase angles, etc. Calibration type adjustments are those that require small changes to the magnitude/phase of a signal, typically within 5% of the magnitude, or within 5 degrees of the phase. The purpose of calibration adjustments is to compensate for errors in the measurement chain. These may be useful for a PDC, especially for a substation PDC, but generally, this function is performed in a PMU. Bulk type phase and magnitude adjustments are those that require large changes to the phase/magnitude of a synchrophasor signal. These are useful, for example, when a signal needs to be referenced across a transformer when the phase identification of the destination system is different (ABC versus ACB) from the source system, or when the quantities are being referenced across a wye-delta (or star-delta) transformer.

2.1.3.2 Library of Test Conditions

Table 2.6: Library of PDC tests

Test No.	PDC Functionality Test
1.	Time Alignment of Data
2.	Data Validation
3.	Data Loss
4.	Data Latency
5.	Reporting Rate Conversion
6.	Format & Coordinate Conversion
7.	Phase & Magnitude Adjustment

IEEE Standard for PDC testing C37.244-2013 specifies the tests that need to be performed on PDCs. From the pool of tests, some of the important tests have been performed at SGDRIL, WSU. Table 2.6 provides the library of test conditions. The descriptions of the functionality tests have been provided in Section 2.1.3.1.

2.1.3.3 Performance of PDC Testing

Two different test beds have been created for testing PDCs. Fig. 2.27 provides the functional schematic diagram of the test bed used for performing PDC tests where data loss due to long distance communication issues has not been tested. This simulates an environment in which the PMU and the PDC are located in the same substation. Fig. 2.28 provides the functional schematic diagram of the test bed used for performing PDC tests where data loss due to long distance communication issues has also been tested. This simulates an environment in which the PMU and the PDC are located in the different substations or the PMU is sending data from a substation to a PDC located in the control center.

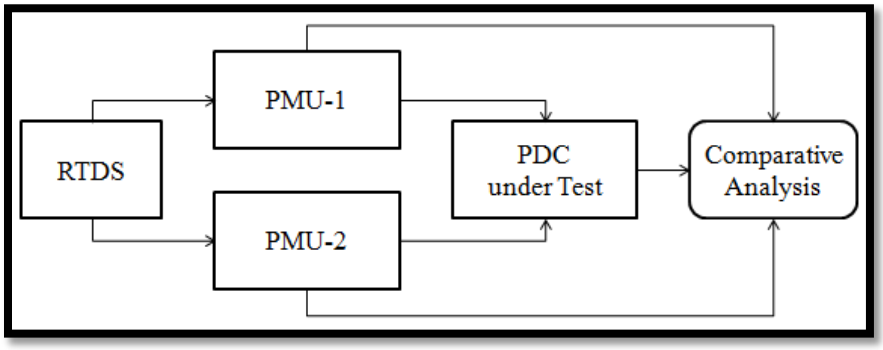

Figure 2.27: Test bed for testing PDCs without communication modeling

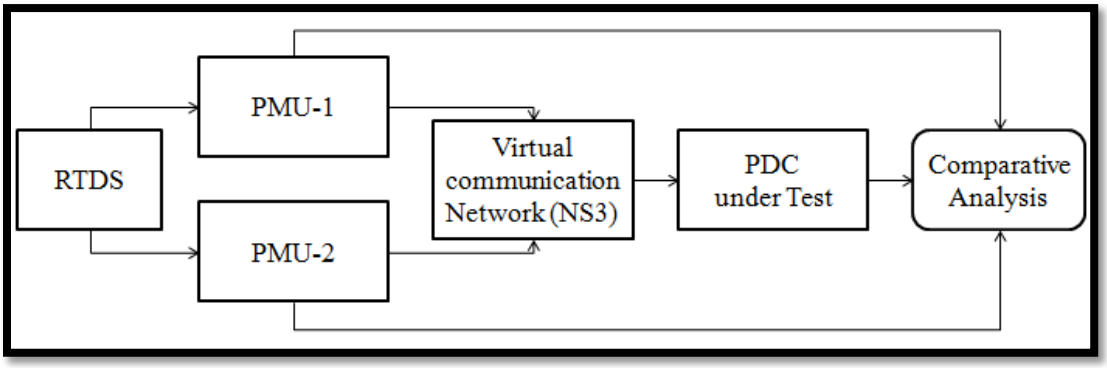

Figure 2.28: Test bed for testing PDCs with communication model

In fig. 2.28, NS3 i.e. Network Simulator 3 has been used to model long distance communication delays and latencies in a system network. NS3 is a discrete-event simulator targeted primarily for research and educational use and is an open-source project. It is the successor to the highly popular NS2, but NS3 has been written from scratch and not derived from NS2. It uses C++ for scripting with python bindings. NS3 supports emulation mode of operation and has the ability to simulate communication issues in real time.

2.1.3.4 Conclusion from Test Results

(A) Discussion on Test-1: Time Alignment of Data

Table 2.7: Test results for time alignment (rate = 30 frames / second)

Time Duration of Data Collection in PDCs	Number of Data Frames Streamed	Number of Time Alignment Errors in PDC-A	Number of Time Alignment Errors in PDC-B
30 minutes	54000	0	0
1 hour	108000	0	0
6 hours	648000	0	0
12 hours	1296000	0	0
24 hours	2592000	0	0

Table 2.8: Test results for time alignment (rate = 60 frames / second)

Time Duration of Data Collection in PDCs	Number of Data Frames Streamed	Number of Time Alignment Errors in PDC-A	Number of Time Alignment Errors in PDC-B
30 minutes	108000	0	0
1 hour	216000	0	0
6 hours	1296000	0	0
12 hours	2592000	0	0
24 hours	5184000	0	0

From the results presented in table 2.7 and 2.8, it can be seen that for different durations and reporting rate of data streaming, collection and archival, the tested PDCs were able to align data w.r.t. the GPS clock time signal referenced to the UTC. Both the test PDCs passed the data time alignment test.

(B) Discussion on Test-2: Data Validation

Table 2.9: Test results for data validation (rate = 30 frames / second)

Level of System Voltage (Simulated using RTDS)	Number of Data Errors in PDC-A	Number of Data Errors in PDC-B
13.8 kV	0	0
138 kV	0	0
230 kV	0	0
500 kV	0	0
760 kV	0	0

Table 2.10: Test results for data validation (date = 60 frames / second)

Level of System Voltage (Simulated using RTDS)	Number of Data Errors in PDC-A	Number of Data Errors in PDC-B
13.8 kV	0	0
138 kV	0	0
230 kV	0	0
500 kV	0	0
760 kV	0	0

For Data Validation Test, decimal points of each data should be identical. Rounding off the data with higher number of decimal points was used to solve this issue. After round off all data validation test with CRC check was performed. From the results presented in table 2.9 and 2.10, it can be seen that for different reporting rate of data streaming, collection and archival, the tested PDCs good performance with data errors. Both the test PDCs passed the data validation test.

(C) Discussion on Test-3: Data Loss

As discussed earlier, data loss has been studied using two different testbeds - one in a small network where the PMU streams data directly to a PDC through a network switch, and the other one in which NS3 (network simulator) is used between the PMU and the PDC to model communication issues in the system network.

Table 2.11 and 2.12 show the results of data loss when the test is carried out on a small network without NS3 simulator.

Table 2.11: Test results for data loss (rate = 30 frames / second)

Time Duration of Data Collection in PDCs	Number of Data Frames Streamed	Number of Data lost in PDC-A	Number of Data lost in PDC-B
30 minutes	54000	0	0
1 hour	108000	0	0
6 hours	648000	0	0
12 hours	1296000	0	0
24 hours	2592000	0	0

Table 2.12: Test results for data loss (rate = 60 frames / second)

Time Duration of Data Collection in PDCs	Number of Data Frames Streamed	Number of Data lost in PDC-A	Number of Data lost in PDC-B
30 minutes	108000	0	0
1 hour	216000	0	0
6 hours	1296000	0	0
12 hours	2592000	0	0
24 hours	5184000	0	0

Table 2.13 shows the results of data loss when the test is carried out on a larger network using NS3 simulator.

Table 2.13: Test results for data loss with network (rate = 60 frames / second)

Time Duration of Data Collection in PDCs	Number of Data Frames Streamed	Number of Data lost in PDC-A	Number of Data lost in PDC-B
1 hour	216000	2203	2131

From Tables 2.11 and 2.12, it can be seen that when a PMU directly streams data to a PDC (such that the data does not need to go through any complex communication network), there is no data loss. However, when the PMU sends data to the PDC via communication networks, there is considerable data loss. For PDC-A, there is 1.02% data loss, whereas for PDC-B, there is 0.986% data loss.

Table 2.14: Test results for data latency

Time Duration of Data Collection in PDCs	Number of Data Frames Streamed	Average Latency for PDC-A	Average Latency for PDC-B
30 minutes	54000	51.1028 ms	51.0054 ms
1 hour	108000	49.5897 ms	49.7183 ms
6 hours	648000	38.8801 ms	49.7628 ms
12 hours	1296000	38.8650 ms	48.6893 ms
24 hours	2592000	38.8903 ms	50.0694 ms

(D) Discussion on Test-4: Data Latency

Table 2.14 shows the data latency when the PMU sends data to a PDC through the communication network as shown in figure 2.28. From the above table it can be seen that for the same test setup, on an average PDC-A performs better than PDC-B.

(E) Discussion on Test-5: Reporting Rate Conversion

Tables 2.15 and 2.16 show the performance of the test PDCs for reporting rate conversion comprising of down-rate conversion from 60 Frames / second to 30 Frames / second and 30 Frames / second to 60 Frames / second.

Table 2.15: Test results for report rate conversion (60 to 30)
(Down-rate conversion from 60 F/s to 30 F/s)

Function Supported in PDC-A	Function Supported in PDC-B
Satisfactory	Satisfactory

Table 2.16: Test results for report rate conversion (30 to 60)

(Up-rate conversion from 30 F/s to 60 F/s)

Function Supported in PDC-A	Function Supported in PDC-B
Satisfactory	Satisfactory

It can be seen from both the above result tables that the test PDCs show satisfactory performance for this test.

(F) Discussion on Test-6: Format & Coordinate Conversion

Tables 2.17 and 2.18 show the performance of the test PDCs for Format & Coordinate Conversion from polar to rectangular and rectangular to polar respectively.

Table 2.17: Test results for format & coordinate conversion (polar to rectangular)

(Polar to Rectangular form)

Function Supported in PDC-A	Function Supported in PDC-B
Satisfactory	Satisfactory

Table 2.18: Test results for format & coordinate conversion (rectangular to polar)

(Rectangular to Polar form)

Function Supported in PDC-A	Function Supported in PDC-B
Satisfactory	Satisfactory

It can be seen from both the above result tables that the test PDCs show satisfactory performance for this test.

(G) Discussion on Test-7: Phase & Magnitude Adjustment

Tables 2.19 and 2.20 show the performance of the test PDCs for phase adjustment of +5 degrees and -5 degrees respectively in the PDCs w.r.t. the phase angle data streamed by the PMU. On the other hand, Tables 2.21 and 2.22 show the performance of the test PDCs for magnitude adjustment of +5% and -5% respectively in the PDCs w.r.t. the magnitude data streamed by the PMU. These adjustments are of high importance when calibration needs to be done at the PDC level.

Table 2.19: Phase angle adjustment (+5 degrees)

Function Supported in PDC-A	Function Supported in PDC-B
Satisfactory	Satisfactory

Table 2.20: Phase angle adjustment (-5 degrees)

Function Supported in PDC-A	Function Supported in PDC-B
Satisfactory	Satisfactory

Table 2.21: Magnitude adjustment (+5%)

Function Supported in PDC-A	Function Supported in PDC-B
Satisfactory	Satisfactory

Table 2.22: Magnitude adjustment (-5%)

Function Supported in PDC-A	Function Supported in PDC-B
Satisfactory	Satisfactory

It can be seen from both the above result tables that the test PDCs show satisfactory performance for this test. All the tests in table 2.6 have been carried out successfully. However, while carrying out the tests, we realized not having performance evaluation threshold criteria for PDCs (like what is available for PMUs) in the IEEE Standard for PDCs C37.244.

2.2 WinIGS-T based Testing Facility

2.2.3 Description

The purpose of this approach is to provide a high fidelity testing and characterization of the performance of PMU devices from several manufacturers (ABB, Macrodyne, Arbiter, GE, SEL, TESLA, etc.). The aim is to answer the following key questions regarding PMU performance:

- How accurate are the currently available PMU devices under different operating conditions (both magnitude and phase with accuracy of 0.001 pu and 0.01 degrees respectively)?
- Augmenting relays with PMU functionality has been proposed. Are modern relays with PMU functionality able to deliver both functions (protection and GPS synchronization) reliably?
- What are the suggested improvements proposed for the next generation of PMU's?
- What is the most appropriate testing framework for evaluating the performance of current PMU devices?

Within this project, we have recognized that PMU testing and performance evaluation is a difficult task, because of the requirement for high accuracy measurements and timing

(timing of a fraction of a microsecond is required). Hence, high accuracy equipment and algorithms have been employed to ensure accurate characterization. Since it is unrealistic to create devices that generate phasors with accuracy of 0.001 pu in magnitude and 0.01 degrees in phase, we developed a different approach: generate waveforms with standard waveform generating equipment, feed them to the PMUs under testing and capture the input of the PMUs with high precision data acquisition systems. In order to compare the phasors provided by the PMU under testing it is necessary to develop a high accuracy phasor computation method. Such a method has been developed and we refer to it as the standard PMU described in a later section. Thus, the proposed testing procedure is based on accurately recording the input of the PMU and processing it with the standard PMU, which is an extremely accurate procedure to compute fundamental frequency phasor with zero leakage spectrum. Subsequently, the output of the standard PMU is compared with the output of the PMU being tested, yielding a performance evaluation of that device.

One specific issue is to study the performance of PMU devices that combine protective relaying functionalities with GPS synchronization, such as the G60, SEL-421, etc. In this project, various fault scenarios are generated by the signal generator, including various fault conditions to which the relay is supposed to respond, testing both the accuracy relay's protective function and the accuracy of its PMU function, answering the question whether relays with PMU functionality are able to combine the two functions accurately. Finally, the utilization of GPS synchronized equipment will most likely be in substations in a multi-vendor environment. It is important in this case to develop methods for comparative testing of GPS synchronized equipment from different vendors. Within the scope of this project, the performance of PMU devices from various vendors has been evaluated.

Regarding PDC performance, of major importance is (a) the ability of the PDC to time-align PMU data and combine them into one stream of data, while minimizing latencies and (b) the ability of the PDC to fully support the standards so that interoperability is achieved. Another desired characteristic is the ability of the PDC to monitor the observed latencies and identify the sources of latency, thus providing useful reports that could be used towards PDC redesign. Finally, it is desired for the PDC to be able to intelligently handle missing data, e.g. by interpolating using available data and assigning larger measurement errors to interpolated data.

2.2.4 PMU Testing

2.2.4.1 Description of approach

In order to accurately test PMU equipment, a measurement accuracy better than one microsecond is needed. However, it must be noted that creating input waveforms of that accuracy requires extremely expensive equipment. Hence, the approach followed in this project is to generate the input signals from inexpensive, and relatively low accuracy equipment and subsequently measure the waveforms in the input of the PMU devices being tested using a data acquisition system with better than one microsecond accuracy (timing) and 0.001 pu magnitude accuracy. Such data acquisition systems are relatively inexpensive and available (unlike equipment that is able to generate input signals of that

accuracy). The end result, however, is the same and accurate testing of the PMU devices is established. The approach is outlined in the sequel.

Fig. 2.29 shows the testing approach followed in this project. The hardware installation suggested in fig. 2.29 has been installed in the Power Systems Control and Automation lab located in the ECE Van Leer building of the Georgia Tech Campus. The signal generator is able to provide a three phase voltage and current of controllable magnitude and frequency as an input to the GPS synchronized device being tested. Also, it is able to simulate unbalanced and faulted conditions. As mentioned above, a very high precision 24 bit, 10Ms/s A/D digitizer, GPS synchronized is used to measure the generated input waveforms. Simultaneously, the relay data are captured through the communication channels of the relay, as shown in fig. 2.29 [8-9].

The accurately measured device inputs and the device recording are supplied to a personal computer for comparison ("Data acquisition computer" in fig. 2.30). The comparison of the two data sets is performed in the program WinXFM. This program is able to accurately compare two sets of data (namely phase difference up to 0.01^{o} and magnitude error up to 0.005%). The overall approach is illustrated in fig. 2.29 and the specific tests are described next.

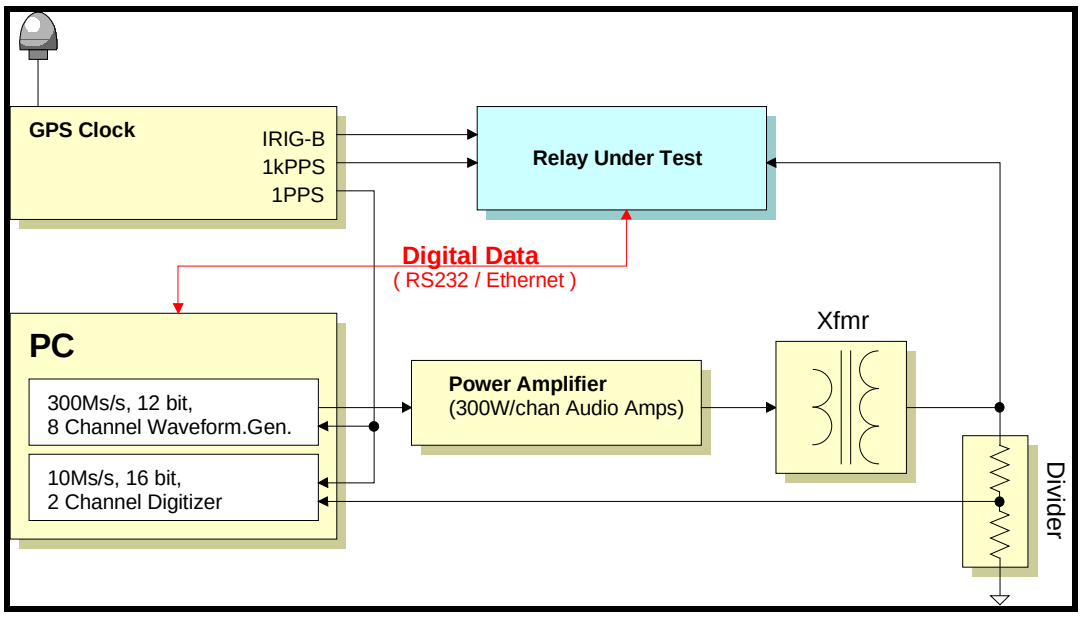

Figure 2.29: Hardware configuration for testing GPS-synchronized IEDs/ PMU

The data acquisition system is illustrated in more detail in fig. 2.31 in block diagram form. It consists of a National Instruments PXI platform with 8 channels of 24 bit A/D converters with maximum sampling rate of 200 ksps.

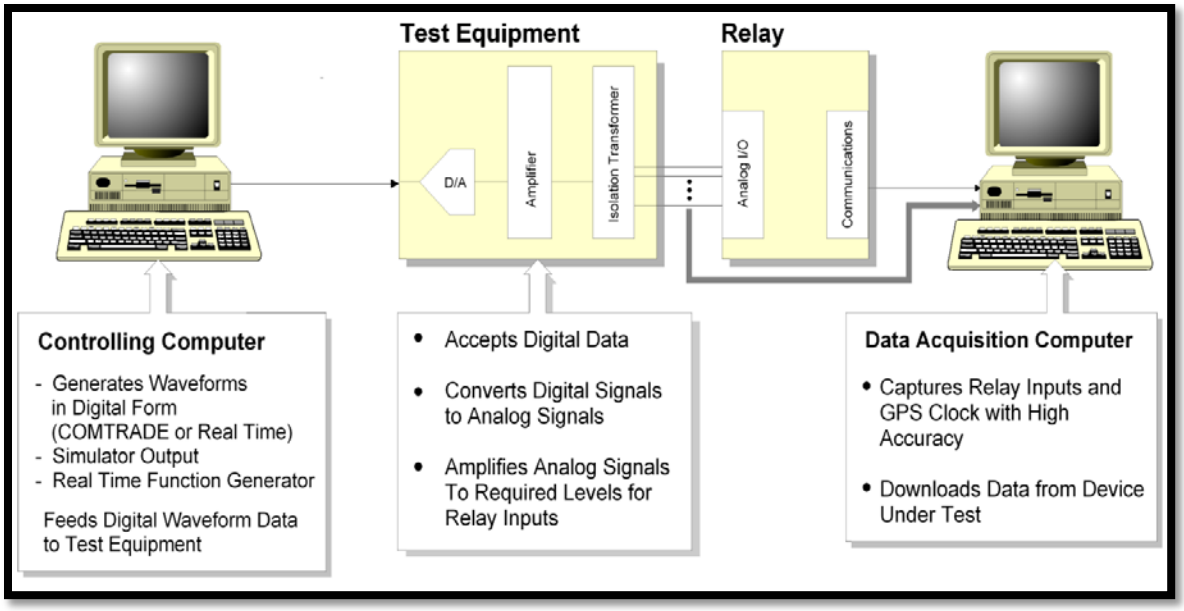

Figure 2.30: Schematic of software architecture for GPS-synchronized IED testing

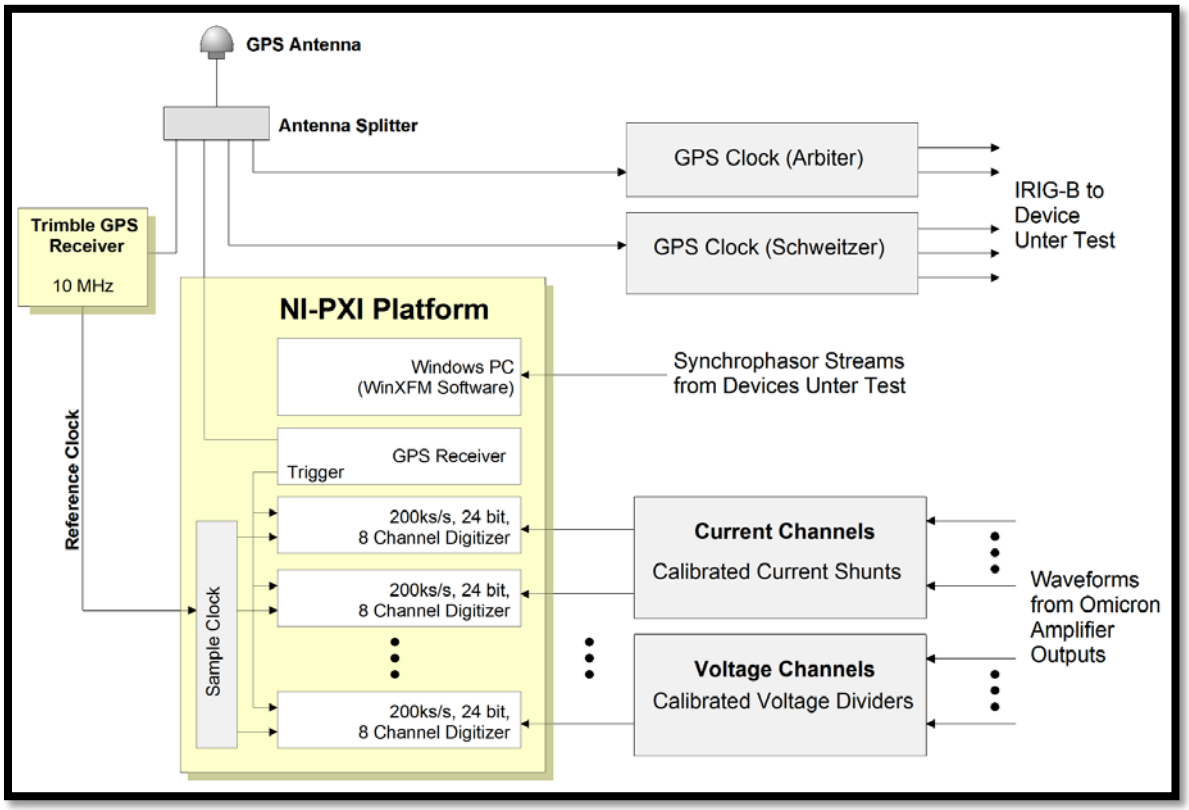

Figure 2.31: Data acquisition system block diagram

The converter sampling clock is obtained from a 10 MHz signal provided from an oven controlled crystal oscillator disciplined to the GPS 1-PPS signal (Trimble Thunderbolt-E unit). The A/D converters are triggered by a clock pulse generated by a second GPS receiver located within the PXI platform. This system achieves UTC synchronized sampling with typical accuracy of less than 100 nanoseconds. As a result the system exceeds the accuracy standard that we set as the goal for this testing.

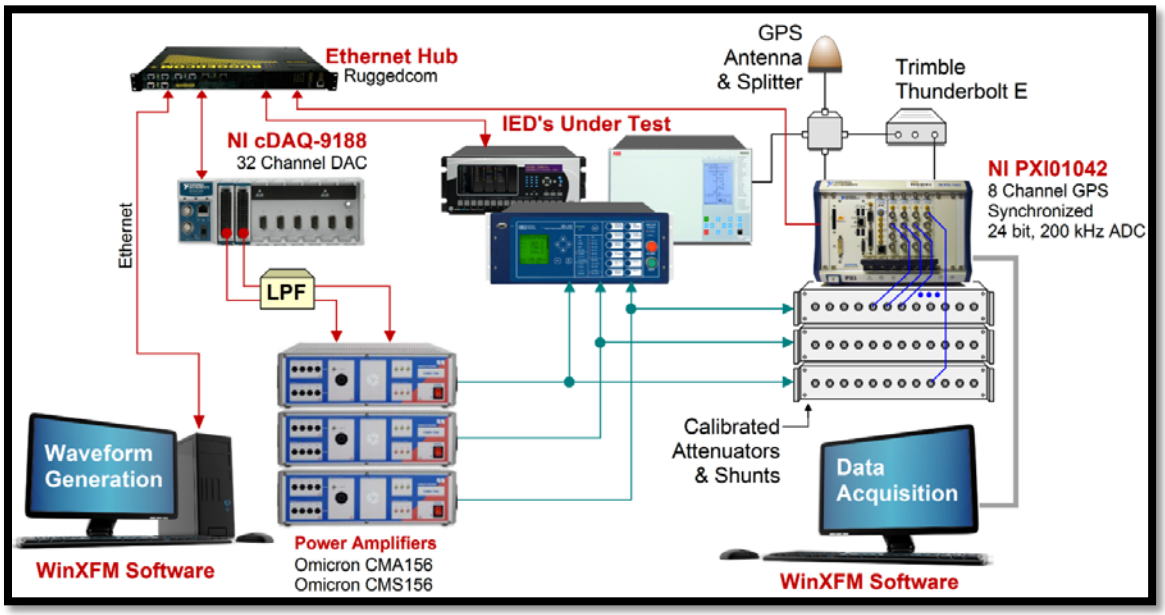

Figure 2.32: Laboratory setup for PMU testing

Figure 2.33: Laboratory setup for PMU testing

The PMU performance evaluation procedure outlined above has been implemented in the laboratory installation of the Power System Control and Automation Lab in Georgia

Tech. The test setup has the capability to generate up to 18 channels of arbitrary voltage and current waveforms at the standard levels for PMU inputs (nominally up to 120 volts and 5A). Generated waveforms can be reproduced from digitized data stored as COMTRADE files or synthesized based on user defined mathematical expressions. For the purpose of validating the phasor stream generated by the device under test, the test setup includes a reference high precision data acquisition system. This system includes 8 digital to analog converter channels with sampling synchronized to UTC time within 100 nanosecond accuracy. An overview of the laboratory setup is shown in fig. 2.32. A photograph of the laboratory is shown in fig. 2.33.

In order to achieve proper characterization of a GPS-synchronized device, the following features are tested:

(a) **Error analysis** of both *timing accuracy* and *magnitude accuracy* over a generally accepted range of operating conditions defined in terms of:

- Frequency
- Frequency Rate of Change
- Voltage Magnitudes
- Current Magnitudes
- Harmonics
- Imbalances

(b) **Ability to communicate** using standard protocols, especially conformity with the IEEE Standard C37.118.

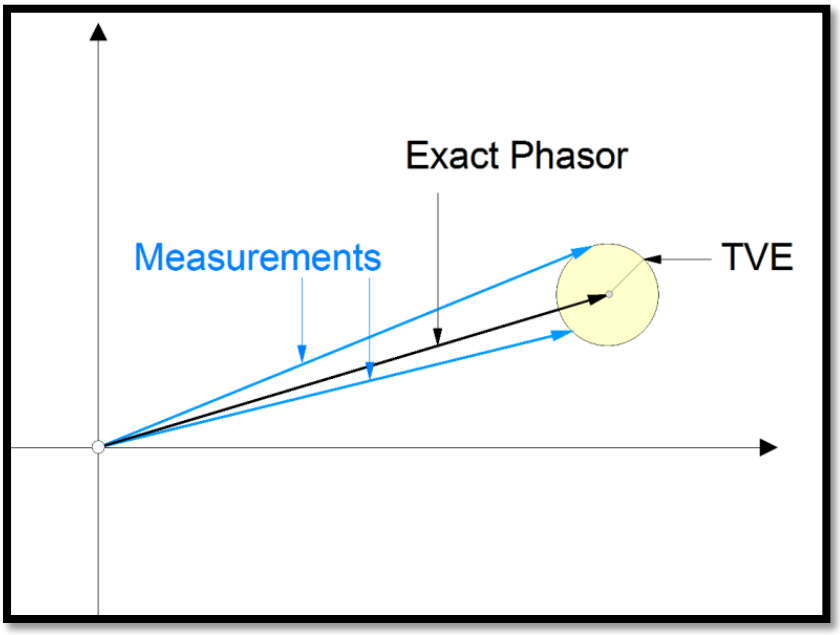

Figure 2.334: Illustration of Total Vector Error (TVE)

There are no standardized tests, but a standard is being developed for that purpose by the NASPI group and adopted by IEEE. Under the IEEE standard, PMU's should be benchmarked by the Total Vector Error (TVE), shown in fig. 2.34. A TVE of 1% includes all phasors that lie within a circle centered at the correct phasor with radius equal to 1% of the exact phasor magnitude. However, this would imply a phase angle error of as much as 0.573^{o}, which severely underestimates the angle measurement accuracy of modern PMU's (which is much greater than the magnitude accuracy).

While we support this standard, it is important to note that our testing goes further than the standard. Specifically, we separately tested PMU performance with accuracy better than 0.001 pu in magnitude and 0.01 degrees in phase (or better than 1 microsecond in timing). In other words our testing is segregated in magnitude and timing.

The specific test procedures are described in terms of metrics that define performance and input test waveforms. The following performance metrics are evaluated for **error analysis:**

- Time or Phase Accuracy
- Magnitude Accuracy
- Frequency Accuracy

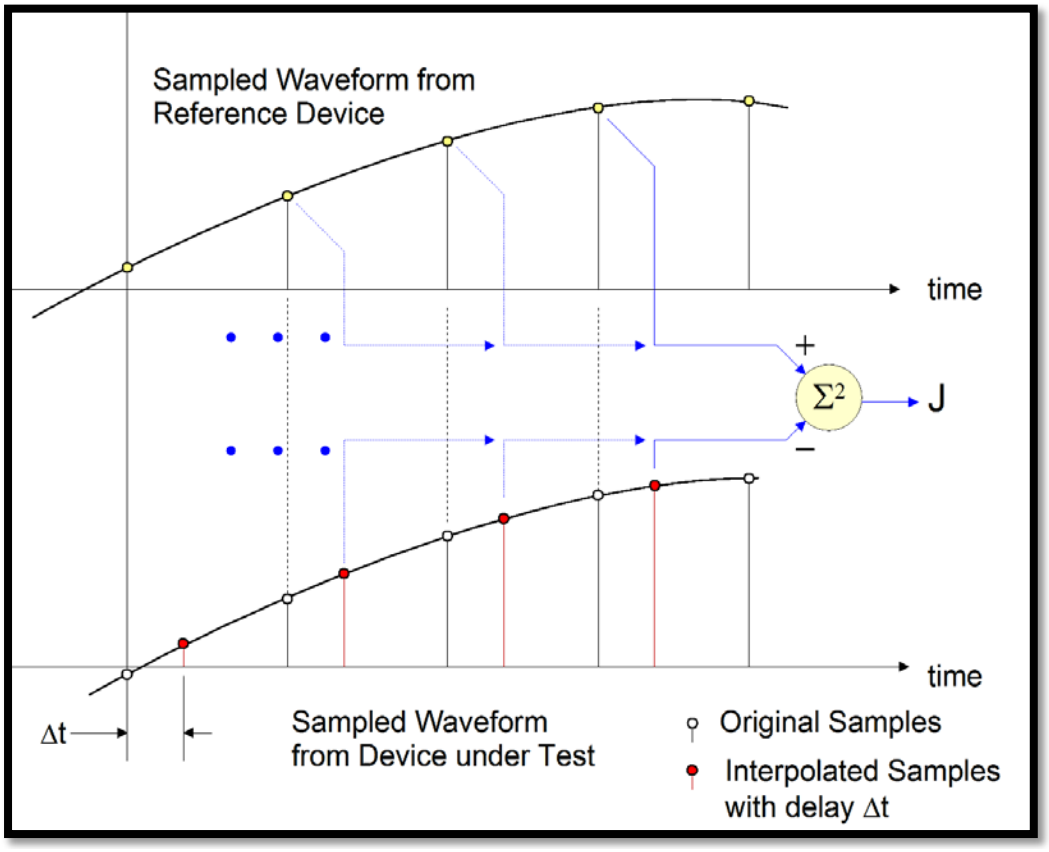

Figure 2.345: Illustration of timing error measurement

Time or Phase Accuracy: The time accuracy of a data acquisition device can be evaluated in two ways, depending on the type of data that can be downloaded from the device under test: (a) If sampled waveform data are available (point on wave data) the time accuracy can be directly determined by comparison of the sample sequence obtained from the device under test to the corresponding sample sequence obtained from the reference data acquisition device. The time accuracy is then extracted from the sample sequences using an estimation based approach.

Let a_k be the sample sequence obtained from the device under test and b_k the sample sequence from the reference device. Let Δt be a variable representing the time error of the device under test, and c a variable representing the magnitude error. The variables Δt and c can be determined by minimizing an objective function $J(\Delta t,c)$ with respect to Δt and c, which is defined as follows:

$$J = \sum_{k=0}^{N} (a_k - (1+c) b_{k-\Delta t})^2$$

where $b_{k-\Delta t}$ represents a re-sampled version of the original sequence from the device under test with time delay Δt. This procedure is illustrated in fig. 2.35.

(b) If the device under test generates phasor data (such as a C37-118 synchrophasor stream) then the timing accuracy is determined by comparing the phasor phase angles. Fig. 2.36 illustrates this procedure.

Magnitude Accuracy: As with time accuracy, the magnitude accuracy is measured either using point on wave data (if available) or phasor data. These two approaches as described in the previous section also provide magnitude accuracy evaluation.

Frequency Accuracy: The frequency accuracy is measured as a percentage difference between the frequency computed by the device under test and the known frequency of the input waveform. Note that the standard PMU also accurately tracks the frequency of the sampled data sequence at a rate equal to the phasor computation rate (up to 60 times per second). Note that tracking waveform fundamental period is necessary for accurate phasor computations. The frequency computation is performed by observing the rate of change of phase angle between successive cycles. Specifically, the following expression yields the fundamental frequency as a function of successively computed phase angle values:

$$f_k = f_0 \left(1 + \frac{\varphi_k - \varphi_{k-1}}{2\pi}\right)$$

where φ_k an φ_{k-1} are two successively computed phase angles, and f_0 is the nominal power frequency.

The **communications metrics** determine whether the device under test complies with the IEEE Standard C37.118 for synchrophasor communications. In addition to time tag,

frequency and phasor magnitude and phase, C37.118 for synchrophasor frames contain additional information such as reference clock accuracy and quality codes, and various user assignable configuration parameters such as station name, phasor, analog and status channel names. Furthermore, most PMUs either contain a built in GPS receiver for obtaining UTC time reference, or accept a time synchronization signal using the IRIG-B standard protocol. Communication metrics are defined which establish that the device under test performs as specified by the relevant standards. Specifically, communications metrics testing includes monitoring the synchrophasor stream accuracy and clock quality codes for various GPS clock states, such as low satellite signal to noise ratio, loss of GPS time lock for various durations, recovery of GPS lock after loss of lock etc. These conditions have been simulated by simply disconnecting the GPS clock (for PMUs with external GPS clock) or by simply putting a metallic object over the GPS antenna to limit the signal for PMUs with internal GPS clock.

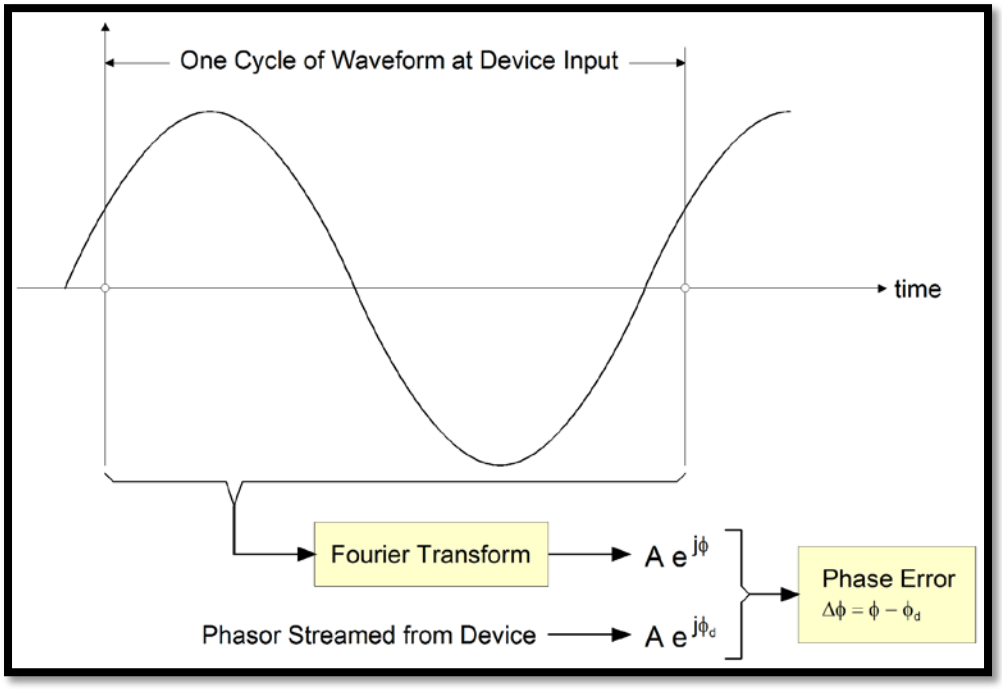

Figure 2.356: Illustration of phase error measurement

2.2.4.2 Test Conditions

In order to fully characterize PMU performance, the following tests are performed:
Timing Accuracy: Determine the timing accuracy of the digitized samples. The accuracy is expressed in terms of microseconds with precision 0.5 microseconds. The timing accuracy directly affects the phase measurement. For each one microsecond error in timing the phase has an error of 0.02 degrees.

Frequency Tests: Determine the frequency error over three different ranges defined below.
Three ranges: Range 1: nominal ± 0.25 *Hz*
Range 2: nominal ± 2.5 *Hz*

Range 3: nominal ± 5 *Hz*

The frequency tests revealed differences among the various manufacturers resulting from the algorithms they use for phase and frequency measurements. At fundamental frequency, all algorithms provided the same result but at off-nominal frequencies, differences did exist.

Frequency Ramp: Determine the frequency ramp error over three frequency ramp rates defined below.

Three ranges: Range 1: 0.05 Hz per sec. for 5 sec.
Range 2: 0.25 Hz per sec. for 10 sec.
Range 3: 0.5 Hz per sec. for 10 sec.

These tests revealed differences among manufacturers. In addition to the algorithms mentioned above, differences existed among various manufacturers because of using different time windows by various manufacturers and different filters.

Voltage Magnitude: Determine the voltage magnitude error in the following voltage magnitude range.

Range: nominal – 25% to nominal +20%

Voltage Phase: Determine the voltage phase error in the following voltage magnitude range.

Range: nominal – 50% to nominal +30%

The phase accuracy is directly related to the timing accuracy. In addition, another source of errors and differences is the front end analog filters used as well as digital filters at the A/D converter level.

Voltage Magnitude Step Change: Determine the voltage magnitude step change error in the following step voltage change values.

- Test 1: nominal – 1% to nominal +1%
- Test 2: nominal – 5% to nominal +5%
- Test 3: nominal – 50% to nominal +10%

Electric Current Magnitude: Determine the current magnitude error in the following two electric current ranges:

- Two Ranges: nominal – 80% to nominal + 100% (non relaying devices)
- Two Ranges: nominal – 80% to nominal + 2000% (relaying devices)

Electric Current Phase: Determine the electric current phase error in the following two electric current ranges.

- Two Ranges: nominal – 80% to nominal + 100% (non relaying devices)
- Two Ranges: nominal – 80% to nominal + 2000% (relaying devices)

Electric Current Imbalance: Determine the electric current imbalance measurement error in the following electric current imbalance ranges (total of four):

- Voltage negative sequence range: zero to 5%
- Voltage zero sequence range: zero to 5%
- Current negative sequence range: zero to 20%
- Current zero sequence range: zero to 20%

Table 2.23: Test conditions for steady state performance

Test Designation	Fundamental Frequency	Total Harmonic Distortion
A-1	60.0 Hz	0
A-2	59.8 Hz	0
A-3	60.2 Hz	0
A-4	59.5 Hz	0
A-5	60.5 Hz	0
A-6	59.0 Hz	0
A-7	61.0 Hz	0
A-8	57.0 Hz	0
A-9	63.0 Hz	0
A-10	55.0 Hz	0
A-11	65.0 Hz	0
A-12	50.0 Hz	0
A-13	70.0 Hz	0
A-14	60.0 Hz	5 %
A-15	59.8 Hz	5 %
A-16	60.2 Hz	5 %
A-17	59.5 Hz	5 %
A-18	60.5 Hz	5 %
A-19	59.0 Hz	5 %
A-20	61.0 Hz	5 %
A-21	57.0 Hz	5 %
A-22	63.0 Hz	5 %
A-23	55.0 Hz	5 %
A-24	65.0 Hz	5 %
A-25	50.0 Hz	5 %
A-26	70.0 Hz	5 %

Testing of Relay/ PMU Devices: One additional test was performed for dual function devices, i.e. PMU capability and relay functions. Presently there are many dual function devices (relays with PMU capability). For these devices, two series of tests have been performed: (a) the GPS-synchronization function has been tested under heavy relaying activity. For this purpose, the input signals to the dual function device has been generated by a power system simulation program and contain multiple fault conditions. The methodology that we have developed can evaluate the timing errors under these conditions. Because in this case the waveforms are not near quasi-steady state, direct timing error measurement are performed instead of phase error measurement. (b) the PMU functions, as defined in the IEEE standard 118, and the relaying functions, as defined by the manufacturer, are tested under several scenarios of multiple fault activity. The following relay functions have been included in the scenarios: (1) phase and ground

distance, (2) overcurrent, (3) directional overcurrent, (4) time overcurrent and (5) out of step. For each of the scenarios the following are determined: (a) accuracy of the PMU reporting function as defined in the IEEE Std C37.118, (b) accuracy of the relay operation as defined in the manufacturers manuals.

Test Signals: A number of test signals has been developed for performing the above mentioned testing procedure. The test waveforms are described below.

Test A: Steady State Tests at Various Frequencies: The test waveform is a constant frequency periodic waveform with various levels of harmonic distortion. For each test, the following parameters are measured: (a) timing error, (b) magnitude error, and (c) frequency error. The input test waveforms are defined in table 2.23.

Test B: Frequency Ramp Tests: The test waveforms are of constant amplitude and with frequency increasing or decreasing at a constant rate of change. For each test, the following are parameters are measured: (a) timing error, (b) magnitude error, and (c) frequency error. The following test waveforms comprise the frequency ramp test set as given in table 2.24.

Table 2.24: Test conditions for frequency ramp test

Test Designation	Initial Frequency & Duration	Ramp Rate & Duration	Final Frequency & Duration	Total Harmonic Distortion
Test B-1	60 Hz, 5 sec	+0.1 Hz/s, 5 s	60.5 Hz, 5 sec	0
Test B-2	60 Hz, 10 sec	−0.1 Hz/s, 5 s	59.5 Hz, 5 sec	0
Test B-3	60 Hz, 10 sec	+0.5 Hz/s, 10 s	65.0 Hz, 5 sec	0
Test B-4	60 Hz, 10 sec	−0.5 Hz/s, 10 s	55.0 Hz, 5 sec	0
Test B-5	60 Hz, 10 sec	+1.0 Hz/s, 10 s	70.0 Hz, 5 sec	0
Test B-6	60 Hz, 10 sec	−1.0 Hz/s, 10 s	50.0 Hz, 5 sec	0

Table 2.25: Test conditions for voltage magnitude test

Test Designation	Fundamental Frequency	Magnitude
C-1	60.0 Hz	50 %,
C-2	60.0 Hz	70 %
C-3	60.0 Hz	130 %
C-4	60.5 Hz	50 %
C-5	60.5 Hz	70 %
C-6	60.5 Hz	130 %
C-7	59.5 Hz	50 %
C-8	59.5 Hz	70 %
C-9	59.5 Hz	130 %

Test C: Voltage Magnitude Tests: A set of constant magnitude and frequency sinusoidal waveforms at various magnitudes and frequencies. For each test, the following are measured: (a) timing error, (b) magnitude error, and (c) frequency error. The following input test waveforms are used (see table 2.25).

Test D: Voltage Magnitude Step Change Tests: The test waveforms are sinusoidal, of constant frequency, and each contains six step magnitude changes 5 seconds apart. For each test, the following are measured: (a) timing error, (b) magnitude error, and (c) frequency error. Table 2.26 shows following input test waveforms defined:

Table 2.26: Test conditions for voltage magnitude step change

Test Designation	Frequency (Hz)	Magnitude (%)	Magnitude (%)	Magnitude (%)	Magnitude (%)	Magnitude (%)	Magnitude (%)
Test D-1	60.0	100	95	50	95	110	100
Test D-2	60.5	100	95	50	95	110	100
Test D-3	59.5	100	95	50	95	110	100

Test E: Electric Current Magnitude Tests: Constant current periodic waveforms of various frequencies, magnitudes, and harmonic distortions. For each test, the following are measured: (a) timing error, (b) magnitude error, and (c) frequency error. The following input test waveforms are used as given in table 2.27:

Table 2.27: Test conditions for current magnitude

Test Designation	Fundamental Frequency	Magnitude (% of Rating)
Test E-1	60.0 Hz	20
Test E-2	60.0 Hz	50
Test E-3	60.0 Hz	200
Test E-4	60.0 Hz	800
Test E-5	60.0 Hz	2000
Test E-6	60.5Hz	20
Test E-7	60.5Hz	50
Test E-8	60.5Hz	200
Test E-9	60.5Hz	800
Test E-10	60.5Hz	2000
Test E-11	59.5Hz	20
Test E-12	59.5Hz	50
Test E-13	59.5Hz	200
Test E-14	59.5Hz	800
Test E-15	59.5Hz	2000

The percentage values refer to the device rated current (1A or 5A).

Table 2.28: Test conditions for voltage and current imbalance tests

		Voltage			Current		
Test Designation	Fund. Frequency	Positive Sequence	Negative Sequence	Zero Sequence	Positive Sequence	Negative Sequence	Zero Sequence
F-1	60.0 Hz	100 %	2 %	2 %	100 %	5 %	5 %
F-2	60.0 Hz	100 %	5 %	5 %	100 %	20 %	20 %
F-3	60.5 Hz	100 %	2 %	2 %	100 %	5 %	5 %
F-4	60.5 Hz	100 %	5 %	5 %	100 %	20 %	20 %
F-5	59.5 Hz	100 %	2 %	2 %	100 %	5 %	5 %
F-6	59.5 Hz	100 %	5 %	5 %	100 %	20 %	20 %

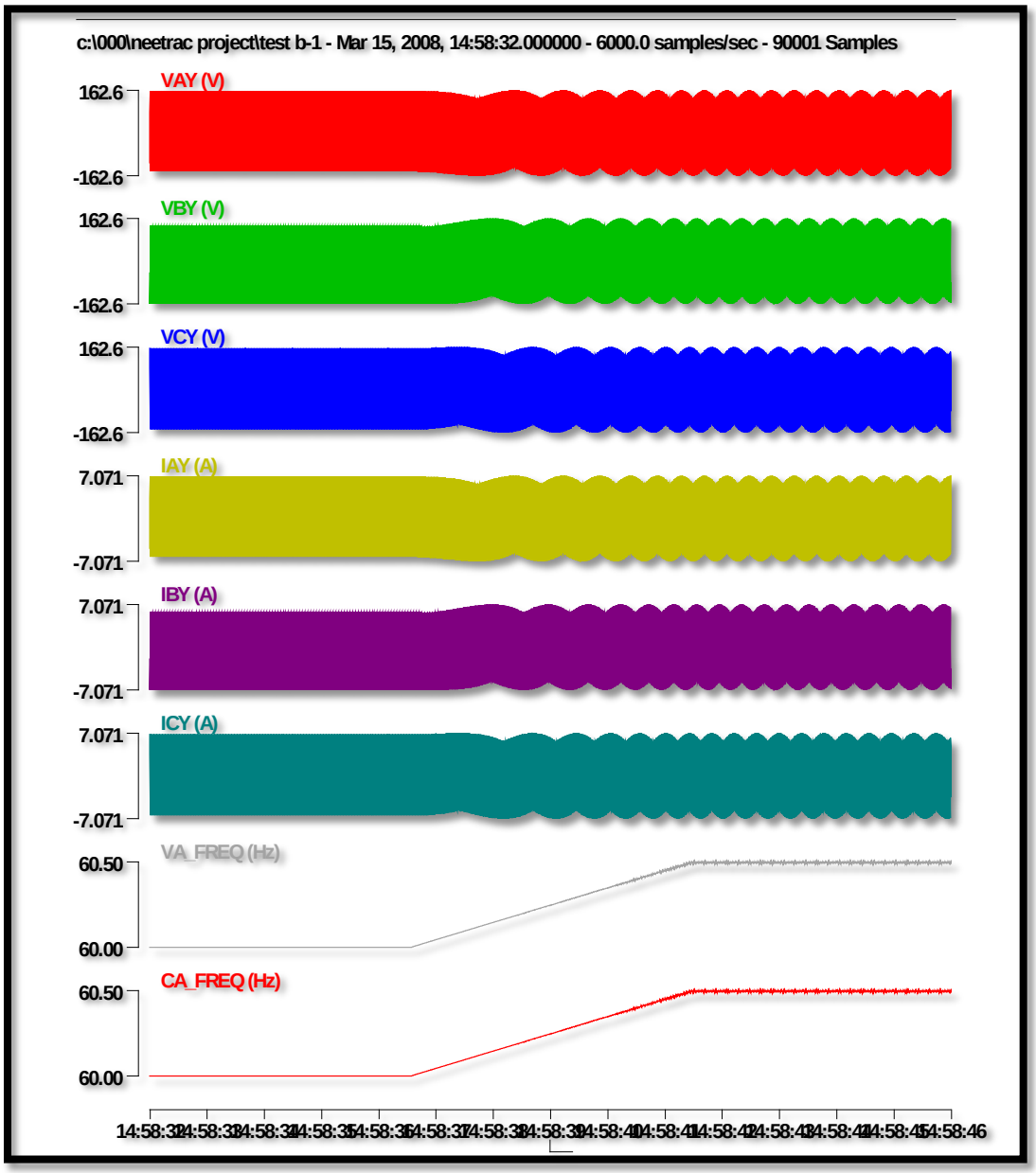

Figure 2.37: Test B-1: Frequency ramp, no harmonics

Test F: Voltage and Current Imbalance Tests: Three phase voltage and current waveforms containing various levels of imbalance defined in terms of sequence components. For each test, the following are measured: (a) timing error, (b) magnitude error, and (c) frequency error. The following input test waveforms are used as shown in table 2.28.

Test G: Composite Waveform Testing (Testing Under Fault Conditions of Relay/PMU Devices): The signals for this test include normal operating conditions interrupted with faults that are cleared. Multiple faults are simulated resulting in exposure of the device under test in multiple faults.

Table 2.29: Performance evaluation - individual phase analysis - test signals A

Test	Magnitude Error (%)			Phase Error (Deg)			Total Vector Error (%)		
	VA	VB	VC	VA	VB	VC	VA	VB	VC
A1	0.006485	0.04042	0.006136	0.222	0.193	0.2	0.388	0.339	0.348
A2	0.01116	0.04095	0.01272	0.232	0.193	0.205	0.187	0.414	0.427
A3	0.009431	0.04502	0.006583	0.236	0.201	0.205	0.412	0.352	0.357
A4	0.01146	0.03887	0.004913	0.227	0.192	0.196	0.396	0.337	0.343
A5	0.01393	0.05303	0.01454	0.248	0.211	0.207	0.434	0.37	0.362
A6	0.02747	0.04741	0.02658	0.268	0.212	0.224	0.467	0.373	0.391
A7	0.03025	0.06655	0.03087	0.233	0.201	0.207	0.407	0.354	0.361
A8	0.07736	0.05603	0.07475	0.243	0.213	0.221	0.425	0.372	0.388
A9	0.07914	0.0116	0.07749	0.251	0.222	0.44	0.385	0.388	0.848
A10	0.117	0.07501	0.124	0.253	0.221	0.232	0.449	0.388	0.41
A11	0.127	0.161	0.128	0.261	0.227	0.229	0.46	0.411	0.405
A12	2.471	2.487	2.479	10.64	10.61	10.63	18.48	18.32	18.45
A13	2.598	2.653	2.623	10.08	10.11	10.11	17.76	17.82	17.82
A14	0.01314	0.06095	0.02507	0.234	0.204	0.2	0.408	0.36	0.349
A15	0.02246	0.05622	0.0199	0.241	0.205	0.215	0.42	0.362	0.375
A16	0.03038	0.06609	0.02924	0.25	0.215	0.224	0.436	0.377	0.391
A17	0.01971	0.05776	0.01979	0.243	0.206	0.214	0.424	0.361	0.374
A18	0.03443	0.07088	0.03346	0.254	0.218	0.226	0.443	0.385	0.395
A19	0.02525	0.06172	0.02284	0.246	0.211	0.222	0.43	0.37	0.387
A20	0.04789	0.08359	0.04753	0.255	0.219	0.228	0.446	0.389	0.398
A21	0.0473	0.08456	0.052	0.253	0.219	0.227	0.443	0.389	0.397
A22	0.04797	0.08444	0.04734	0.255	0.219	0.228	0.445	0.389	0.399
A23	0.107	0.08478	0.109	0.271	0.233	0.246	0.478	0.407	0.436
A24	0.04741	0.08384	0.04811	0.251	0.215	0.226	0.438	0.382	0.395
A25	2.528	2.555	2.5	10.62	10.59	10.6	18.45	18.38	18.41
A26	2.637	2.51	2.432	10.3	10.43	10.58	17.98	17.83	17.91

For limiting the size of this report, the signal waveforms are not included (they are however available in electronic form - in COMTRADE format). As an example, the waveform for Test B-1 case is depicted in fig. 2.37 for Freq=60Hz for 5 secs, ramping rate +0.1 Hz/sec for 5 secs, Freq=60.5Hz for another 5 seconds.

2.2.2.3 Performance of PMU testing

Table 2.30: Performance evaluation - positive sequence - test signals A

Test	Maximum Magnitude Error (%)	Maximum Phase Error (Deg)	Maximum TVE (%)	Frequency Error (Hz)
A1	0.04042	0.222	0.388	0.000284
A2	0.40400	0.339	0.357	0.000187
A3	0.04502	0.236	0.412	0.000147
A4	0.03887	0.227	0.396	0.000193
A5	0.05303	0.248	0.434	0.000537
A6	0.04741	0.268	0.467	0.000133
A7	0.06655	0.233	0.407	0.000364
A8	0.07736	0.243	0.425	0.000633
A9	0.07914	0.44	0.848	0.000289
A10	0.12400	0.253	0.449	0.000614
A11	0.16100	0.261	0.46	0.000437
A12	2.48700	10.64	18.48	0.000686
A13	2.65300	10.11	17.82	0.000685
A14	0.06095	0.234	0.408	0.000391
A15	0.05622	0.241	0.42	0.000116
A16	0.06609	0.25	0.436	0.000213
A17	0.05776	0.243	0.424	0.000383
A18	0.07088	0.254	0.443	0.000597
A19	0.06172	0.246	0.43	0.000108
A20	0.08359	0.255	0.446	0.000464
A21	0.08456	0.253	0.443	0.000546
A22	0.08444	0.255	0.445	0.000428
A23	0.10900	0.271	0.478	0.000649
A24	0.08384	0.251	0.438	0.00042
A25	2.55500	10.62	18.45	0.000647
A26	2.63700	10.58	17.98	0.000688

For keeping the report concise, the detailed test results are not included here. Instead we provide representative performance report for one device without identifying the device. You will note that the performance data are identified by the test, i.e. test A-1, B-3, etc. The performance data are expressed in terms of magnitude error, phase error and total

vector error for individual phase phasors and for positive sequence phasor as well as frequency error. Only representative test results are presented in table 2.29 to table 2.32.

Table 2.31: Performance evaluation - individual phase analysis - test signals B

Test	Phase Error (Deg)			Magnitude Error (%)			Total Vector Error (%)		
	VA	VB	VA	VB	VC	VC	VA	VB	VC
B1	0.01398	0.05226	0.01442	0.234	0.202	0.2007	0.409	0.354	0.361
B2	0.01854	0.04265	0.01714	0.226	0.193	0.202	0.395	0.338	0.353
B3	0.159	0.197	0.16	0.262	0.231	0.233	0.466	0.419	0.414
B4	0.114	0.08605	0.116	0.277	0.241	0.254	0.484	0.422	0.443
B5	2.74	2.796	2.736	10.21	10.24	10.25	17.76	17.82	17.82
B6	2.471	2.5	2.443	10.61	10.58	10.59	18.42	18.37	18.4

Table 2.32: Performance evaluation - positive sequence - test signals B

Test	Maximum Magnitude Error (%)	Maximum Phase Error (Deg)	Maximum TVE (%)	Frequency Error (Hz)
B1	0.05226	0.234	0.409	0.000393
B2	0.04265	0.226	0.395	0.008391
B3	0.19700	0.262	0.466	0.000379
B4	0.11600	0.277	0.484	0.03835
B5	2.79600	10.25	17.82	0.000382
B6	2.50000	10.61	18.42	0.000682

2.2.2.4 Conclusion from Test Results

The tests reveal that the performance of the various PMU tested are excellent under steady state conditions and near nominal frequency. The tested PMUs meet the IEEE Std permissible error of total vector error. However under transient and off nominal frequency there is great variability among the various manufacturers and the errors can be quite high. All performance data do not identify the specific device tested.

3 Validation and Testing of Synchrophasor Applications

3.1 Voltage Stability Algorithms Based on Synchrophasor Data

3.1.1 Introduction to Voltage Stability

Until the last two decades, power systems could afford to be overdesigned. But now due to the increasing loads, environmental limitations on the expansion of transmission system and high competition amongst the transmission utilities, the power systems are being pushed to their stability limits. Due to these factors, they now operate under severely stressed conditions. This in turn has increased the chances of the power system to exhibit unstable behavior that is often characterized by voltage instability, sometimes even leading to a total collapse (or blackout). As numerous voltage instability incidents have occurred around the globe in recent years, voltage stability studies have gained momentum. Voltage stability has now become one of the major concerns in the planning and operation of all power systems.

A. Definitions of Voltage Stability

There have been several revisions in the definition of voltage stability and voltage collapse over a period of years [10]. Following are the accepted definitions –

(i) According to IEEE [1990]: Voltage collapse is the process by which voltage instability leads to loss of voltage in a significant part of the system.

(ii) According to CIGRE [1993]: Voltage instability is the absence of voltage stability, and results in progressive voltage collapse (or increase).

(iii) According to Kundur [1994]: Voltage stability is the ability of a power system to maintain steady acceptable voltage at all buses in the system at normal operating conditions, and after being subjected to a disturbance.

(iv) According to IEEE / CIGRE Joint Task Force [2004]: Voltage stability refers to the ability of a power system to maintain steady voltages at all buses in the system after being subjected to a disturbance from a given initial operating condition. It depends on the ability to maintain / restore equilibrium between load demand and load supply from the power system. Instability that may result occurs in the form of progressive fall or rise of voltages of some buses. Voltage collapse is the process by which the sequence of events accompanying voltage instability leads to a blackout or abnormally low voltages in a significant part of the power system.

B. Classification of Voltage Stability –

Based on the nature of the phenomenon of voltage stability (or instability), following classification has been advocated in [10] –

(i) Large Disturbance Voltage Stability – Refers to system's ability to maintain steady voltages after large disturbance such as system faults, loss of generation, or circuit contingencies.
(ii) Small Disturbance Voltage Stability – Refers to system's ability to maintain steady voltages when subjected to small perturbations such as incremental changes in system load.
(iii) Short Term Voltage Stability – Refers to a disturbance period of the order of several seconds.
(iv) Long Term Voltage Stability – Refers to a disturbance period of the order of several or many minutes.

C. A Brief Note on Application of Synchrophasor Technology for Voltage Stability Assessment –

The event of August 14, 2003 blackout in the north eastern United States and parts of Canada that affected almost 50 million people, emphasized the use of time-synchronized recording devices in the Report of US-Canada Power System Outage Task Force. Such synchrophasor devices like Phasor Measurement Units (PMUs) enable continuous wide area visualization of a power system network in the form of time stamped voltage and current phasors.

Following are some of the benefits that Synchrophasor technology provides as compared to the traditional SCADA technology –

(i) PMUs can provide synchrophasor data at the rate of 30/60/120 phasor datasets per second as compared to 1 dataset in 4 seconds as provided by SCADA technology.
(ii) Synchrophasor technology direct measurement of voltage and current angles at the bus or a branch using time reference 'UTC' obtained from GPS satellite clocks, and thus there is no need for calculating these values using a state estimator as required if SCADA technology is used.
(iii) Synchrophasor technology provides a wide area view of the power system in the form of time synchronized measurements from different geographically located substations, as compared to local non-time synchronized measurements obtained using SCADA technology.

Hence, synchrophasor technology enables a good assessment of power grid stress like voltage instability.

3.1.2 Testbed for performing online simulation of voltage stability algorithms

This section gives a brief description of each of the hardware devices and software used in the test bed at Smart Grid Demonstration & Research Investigation Lab (SGDRIL) at WSU, along with each of their potential applications [5].

Real Time Digital Simulator

Real Time Digital Simulator (RTDS) is a power system simulator that simulates a power system built in RSCAD user interface software in real time. The RTDS works on the parallel processing technology of digital signal processors and executes the program developed on its processors. The RTDS not only calculates and shows the electrical output values in the runtime software, but also produces scaled output signals (digital as well as analog) through the output interface cards incorporated into its system. The RTDS present in the SGDRIL, WSU, consists of one rack with three Giga Processor Cards (GPCs) – for processing all computations in real time; one Giga Transceiver Workstation Interface Card (GTWIF) – for interfacing the RSCAD user software with the GPC cards of the RTDS; one Giga Transceiver Digital Input Card (GTDI) – for taking in input digital signals from external devices like relays; one Giga Transceiver Front Panel Interface card (GTFPI) – for taking in input digital signals and giving out output digital signals from and to hardware devices like relays; three Giga Transceiver Analog Output Card (GTAO) – for providing analog output signals to hardware devices like PMUs for measuring electrical quantities; one Giga Transceiver Analog Input Card (GTAI) – for taking in analog input signals from hardware devices; one Giga Transceiver Network Interface Card (GTNET) – for interfacing a number of different network protocols with the RTDS simulator; and one Giga Transceiver Synchronization Card (GTSYNC) – for synchronizing the RTDS simulation time step to an external time reference like the GPS clock.

GPS Clock

A GPS clock provides the time synchronization signal to all the synchrophasor devices, so that all these devices are in time sync with each other and the data time stamping is done simultaneously irrespective of their geographical location. The requirement of a GPS clock to send such time signals is that it must “lock” with 4 GPS satellites through the GPS antenna. This kind of precise time synchronization amongst all the devices is critical for detailed event analysis. In SGDRIL, there are two GPS clocks – SEL-2407 and PONOVO PGPSO2. These devices provide IRIG-B type time pulse outputs for the synchrophasor device IRIG-B inputs.

Relays / PMUs / DFRs

These are the Intelligent Electronic Devices (IEDs) that form the heart of the smart grid test bed. Advancements in high speed and reliable microprocessor based programmable relays in conjunction with advanced communication technology embedded in such devices make monitoring and control tasks much more efficient than their predecessors. Many of these relays have fault finding feature, which reduces the fault finding time by about 50%. Many relay manufacturers also provide the synchrophasor measurement module (i.e. a PMU) along with the relay module, which means the monitoring as well as control module, both are in the same device. Many of these devices have event recording feature for post event analysis purposes. In the test bed, there are different kinds of relays, meant for generator protection, motor protection, transmission line protection,

transformer protection, capacitor bank protection, reactor protection, etc. Relays/PMUs in the test bed include SEL-351 (2 nos.) with synchrophasor measurement feature – for non-directional and directional overcurrent protection, enhanced breaker monitoring, pilot protection scheme, autoreclosure control, and under-frequency loadshedding; SEL-387 (1 no.) – for multi-winding current differential protection, overcurrent protection, restricted earth fault protection; SEL-421 (2 nos.) with synchrophasor measurement feature – for high speed distance protection, directional overcurrent protection, for pilot protection scheme, autoreclosure control, and breaker failure monitoring and control; GE-D60 (1 no.) with synchrophasor measurement feature – for 5-zone quad or mho type distance protection, directional overcurrent protection, multiple standard pilot protection schemes, single pole or three pole tripping applications, 4-shot autoreclosure control, synchronism check for dual breaker operation, out of step tripping and power swing blocking operations; MICOM Alstom P847 (1 No.) – mainly for synchrophasor measurement purpose; and TESLA 3000 disturbance recorder from ERLphase (1 No.) with synchrophasor measurement option – mainly for recording power system data in three domains: high speed transient faults (in seconds), low speed dynamic swing (in minutes), and continuous trend (10 seconds to 1 hour intervals).

Current & Voltage Amplifiers

The RTDS produces low level signals at its output ports (as mentioned earlier in II. A) These low level signals are inadequate to trigger the functioning of the Relays, PMUs and DFRs (except for the ones manufacture by SEL, which have a special low level interface that can accept low level signals for its operation). Thus these signals need to be amplified to get the voltage and current within the acceptable range of each device for it to function properly. In SGDRIL, WSU, there is one current amplifier and one voltage amplifier from PONOVO. The current amplifier has 6 output current channels of range 0-30A with maximum output power of 210VA, and has a typical current accuracy of < 0.1%. The voltage amplifier has 6 output voltage channels of range 0-250V with a maximum output power of > 75VA, and has a typical voltage accuracy of < 0.1%.

Phasor Data Concentrator

A Phasor Data Concentrator (PDC) aggregates synchrophasor data from a number of PMUs and also from PDCs at the lower tier of data acquisition. Aggregated data will be correlated with identical time-tags to create a system wide measurement set and archived to retrieve and use for future work. PDC has additional functions as well. It performs real-time data quality checks and calculations involving high data acquisition rates such as 30 samples per second or higher like 120 samples per second. Since real-time data quality checks and calculations should be done before the next data set arrive, the speed of performance must be very quick. Some PDCs can down-sample stored data to feed them directly to applications such as SCADA that use data at slower sample rates. A PDC is abided by streaming protocol standards such as IEEE C37.118 for both the phasor data input and the combined data output stream to interface with data-using applications. PDCs are available as hardware as well as software. The PDC present in the test bed of SGDRIL is of both types – hardware as well as software. The software PDC is SEL-5073 with integrated data archiving feature that runs on Microsoft Windows based computing

platform. Data can be archived on a continuous basis or on the basis of predefined triggers. This software PDC has the capability of acquiring synchrophasor data from more than 200 PMUs and supports message rates of 240 messages per second. It can send concentrated synchrophasor data to 6 clients at the higher level of monitoring and control. The hardware PDC in SGDRIL is SEL-3373 with integrated data archiving feature. There are two main differences between the hardware PDC and the software PDC. The hardware PDC allows saving of all PMU data on the solid-state drive (SSD) in the secure database. This ensures that no PMU data is lost if communication with the substation is disrupted. This is a clear advantage over the software PDC. However, the other point of difference between the two types of PDCs is that unlike the software PDC, the hardware PDC can acquire synchrophasor data from up to a maximum of 40 PMUs at the same message rate of 240 messages per second (specific to SEL PDC).

Synchrophasor Visualization Software

Many a times, it becomes important to have a visual interpretation of the synchrophasor data to see the trends of the different electrical parameters in real time. SEL SynchroWAVe Central Software SEL-5078 is used to translate synchrophasor data into visual information, thus providing better situational awareness. Synchrophasor data can also be archived for power system analysis.

Synchrophasor Vector Processor

As attempts are being made to make the power grid “smarter”, a lot of importance is being given to real time control of power system on the basis of real time system monitoring. SEL-3378 Synchrophasor Vector Processor (SVP) is a Programmable Logic Controller (PLC) like real time control device which takes in synchrophasor data as its input (either from PDCs, or directly from the PMUs) and outputs control actions, based on the control algorithm in the SVP (to the PDCs, Relays or other intelligent control devices) for wide area protection and control of the power system. The SVP has the ability to identify power system oscillations with preconfigured modal analysis; measure voltage, current, phase angle, real and reactive power; improve the efficiency of the system by optimizing voltages and minimizing loop flows; and control circuit breakers, and/or static VAR compensators based on the control algorithm. Thus, the SVP is a very powerful tool in detecting and controlling the stability of a power system. Another application of this device is for measurement of the states of the power system. It can screen bad data obtained from a station and then send the true data to the Energy Management System (EMS). Additionally, it can also calculate the state vectors of the surrounding stations so as to provide measurement redundancy. Apart from control, the SVP can also be used to generate alarms to the system operators if the set threshold limits of the electrical parameters are violated. In SGDRIL, presently the SVP is primarily being used for identifying and controlling voltage instability in real time at one or more buses in the test case power system.

Substation Automation Computer

SEL-3354 is a robust, computer CPU hardware designed to operate in the harsh environment of a substation. It can have either Windows or Linux as the operating

system. It doesn't have a fan or as such, any moving parts. It is designed to withstand 15 kV electrostatic discharge, overcurrent, dielectric strength, radiated emissions, fast transients, and pulse magnetic field disturbances. It meets IEEE 1613, IEEE C37.90, and IEC 60255 Protective Relay Standards. A field-programmable gate array (FPGA) provides an extra level of computer system reliability with a programmable system monitor interface and alarm configuration. If this hardware CPU is connected to a video monitor, keyboard, and mouse, it can be used to provide a human-machine interface (HMI) for alarm annunciation, local indication, control, and configuration. This hardware has a 4GB RAM and a 60GB or 120 GB solid state drive storage and can be connected to various local peripherals and high-speed network interfaces with three 10/100BASE-T Ethernet (fiber optional), six USB, and up to 16 EIA-232/EIA-485 ports. Several software programs can be installed in SEL-3354 so as to interface it with the Intelligent Electronic Devices (IEDs) installed in the substation. This device can thus be used to make relay settings, gather, view, and analyze event reports generated by substation relays. It can also be used to forward information to multiple master data users, such as SCADA. In SGDRIL, this hardware device has been used to support various interfacing software programs required for communication with relays/PMUs, PDC, and SVP.

NS3: NS3 is a discrete event communication network simulator. In this work, we use NS3 to deliver data between control center and substation while emulating delays due to processing, transmission, propagation and queuing encountered in a real communication network.

Integration of all the software and hardware devices for carrying out online simulation of voltage stability algorithm

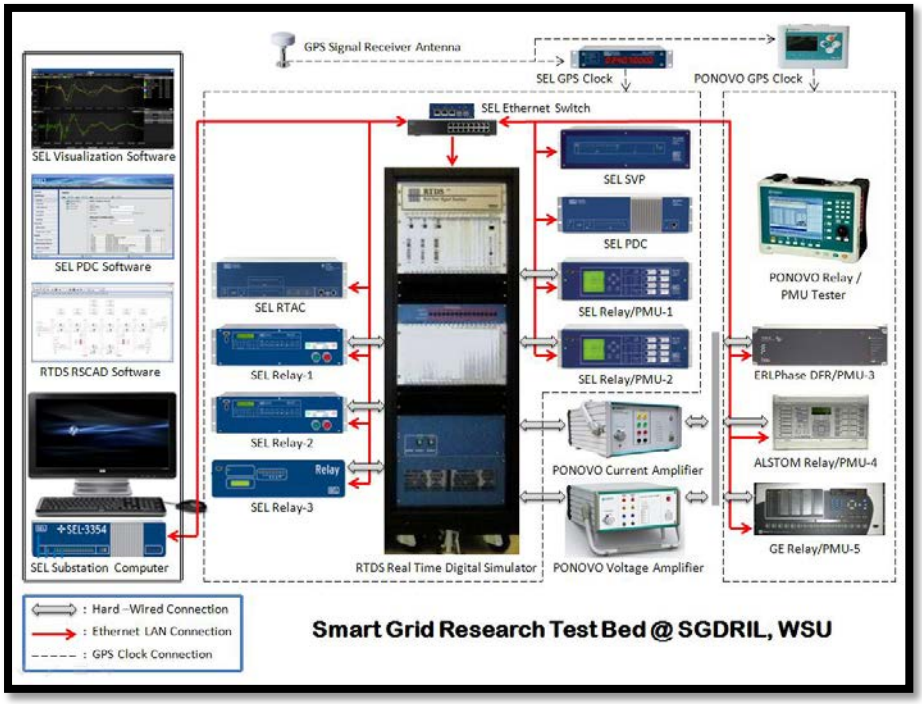

Figure 3.1: Smart grid test bed for simulation of voltage stability algorithm

All the hardware and software programs described in the previous section have been integrated to form a smart grid test bed, which has the capability of supporting real time hardware-in-loop simulations and synchrophasor device testing. Fig. 3.1 shows the architecture of the interconnections (communications and hard wired) amongst the various devices. The computer supports all kinds of softwares (interfacing and simulation) and is connected to the Ethernet switch (hub) so as to communicate with all other devices present in the test bed. The relays / PMUs, SVP are all connected through Ethernet connections to the Ethernet switch for communication purpose. The relays / PMUs are connected to the analog and/or digital output ports of the RTDS to receive low level signals obtained during the real time simulation of the system built in RTDS using RSCAD. Those relays which cannot operate using low level signals have been provided with voltage and current amplifiers, which amplify the signals suitably. The relays / PMUs, RTDS, PDC, and SVP have all been synchronized to the UTC using the GPS Clock. The PDC and SVP can get data from the relays / PMUs.

3.1.3 Performance of online simulations of voltage stability algorithm

The overall functional block diagram of the smart grid test bed with the communication network topology used for an IEEE test case and the substation level views are shown in fig. 3.2. The substation view of slack bus representing node 0 in the communication network shows a PDC concentrating local PMU voltage phasor measurement and sending them to the monitored substation through NS3 emulated communication network. The substation view of this monitored bus representing a node in the communication network shows a PDC concentrating data from the local PMU and receiving voltage phasor from slack bus through NS3. The arrangement of obtaining slack bus measurements is essential as the power flow angle of the monitored bus w.r.t. the slack bus angle can only be obtained if its synchrophasor angle (which are referenced to the UTC) is adjusted with that of the slack bus. Both the PMUs are interfaced with the RTDS to receive measurement signals. The data retrieval script retrieves the required data from the database and feeds it to the algorithm running on the substation computer. The substation computer computes the VSAI and sends it to the control center for visualization through the emulated communication network.

For online simulation purpose using the above mentioned test bed, a real time voltage stability algorithm [5] has been coded in C-language and run on Linux platform in the Substation computer at the monitored bus in each of the tested systems (IEEE-14 Bus system and IEEE-30 Bus system). It has been found that the algorithm runs extremely fast with a guaranteed time step of ≈ 163 microseconds, thus making it highly suitable for real time voltage stability monitoring. As this algorithm is meant for voltage stability monitoring of just the substation that is equipped with a PMU, hence there are no scalability issues.

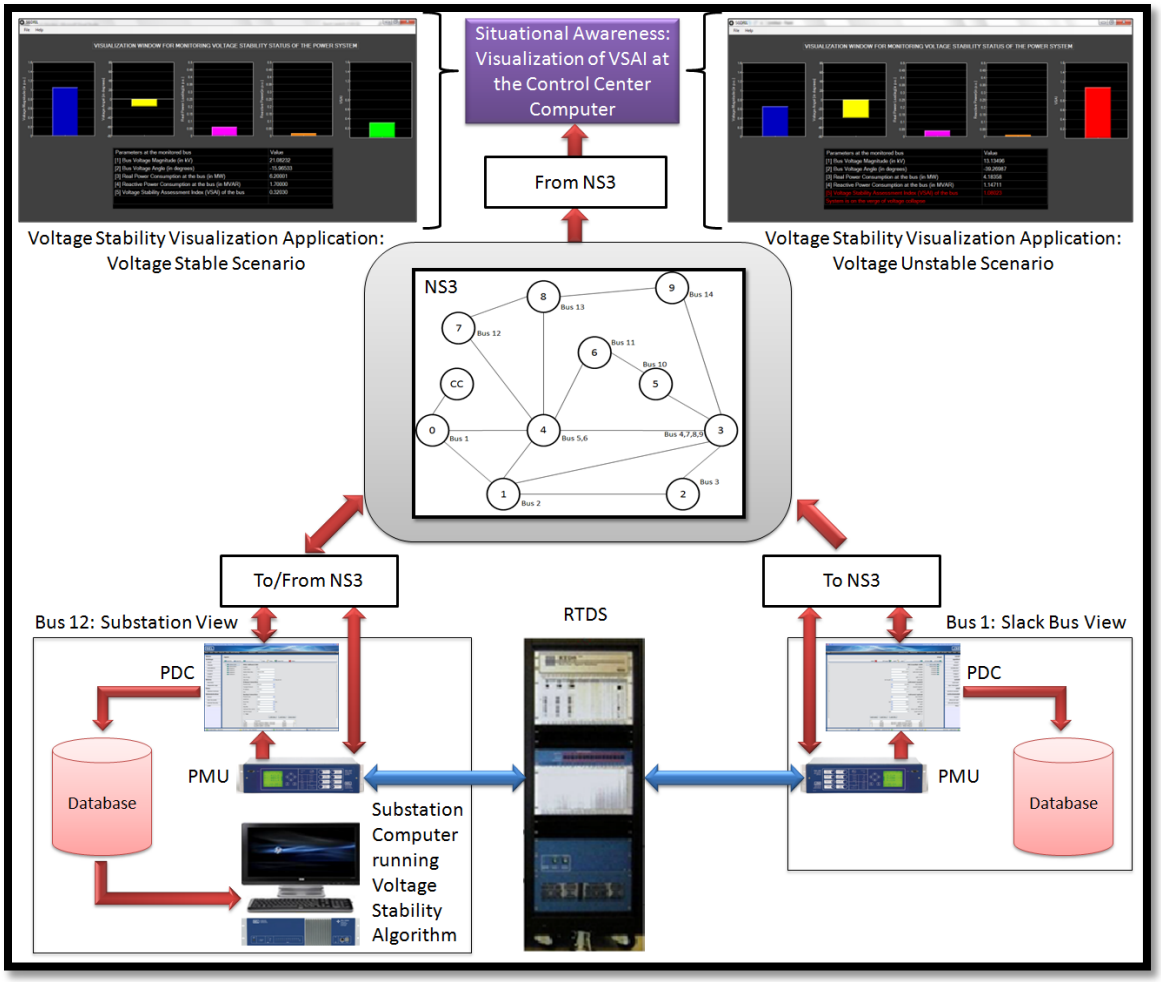

Figure 3.2: Functional block diagram for simulation of voltage stability algorithm

3.1.3.1 Simulation of a possible voltage collapse scenario in an IEEE-14 Bus test case using the Real Time Test Bed

The IEEE-14 Bus test case has been modeled in RSCAD, in which Bus-12 has a PMU for real time monitoring of voltage stability.

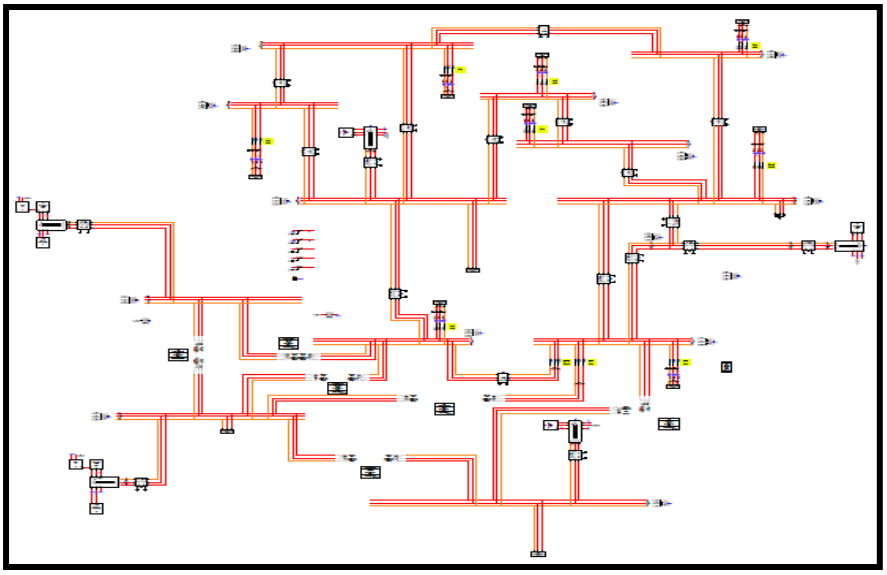

Figure 3.3: IEEE-14 bus test case modeled in RSCAD for real time simulation

Table 3.1: Series of events leading to voltage collapse in IEEE-14 bus test case

Event No. & Time	Event Description
1 at t=25s	Load at Bus-9 increases such that the real power consumption is 44.9 MW and the reactive power consumption is 25.2 MVAR. (Base Case: 29.6 MW & 16.7 MVAR)
2 at t=35s	Load at Bus-10 increases such that the real power consumption is 24.9 MW and the reactive power consumption is 16 MVAR. (Base Case: 9.1 MW & 5.9 MVAR)
3 at t=45s	Load at Bus-14 increases such that the real power consumption is 24.9 MW and the reactive power consumption is 8.3 MVAR. (Base Case: 15 MW & 5.1 MVAR)
4 at t=55s	Load at Bus-11 increases such that the real power consumption is 26.9 MW and the reactive power consumption is 11.5 MVAR. (Base Case: 3.6 MW & 1.9 MVAR)
5 at t=65s	Inverse Time Over-current relay (hardware relay) trips the transmission line connecting Bus-13 and Bus-6 due to loading of the line above the set pick up value.
6 at t=75s	Load at Bus-12 increases such that the real power consumption is 11.9 MW and the reactive power consumption is 3.1 MVAR. (Base Case: 6.2 MW & 1.7 MVAR)
7 at t=85s	Inverse Time Over-current relay (hardware relay) trips the transmission line connecting Bus-12 and Bus-6 due to loading of the line above the set pick up value.

Table 3.1 shows the series of events that have been simulated using the RSCAD test case in RTDS for a possible voltage collapse scenario, assuming that initially the system is at base case.

The Event-7 finally leads to a voltage collapse. Fig. 3.4 shows the voltage magnitude at the Bus-12 and fig. 3.5 shows the voltage angle at the Bus-12, as simulated in real time in RTDS runtime. From fig. 3.4, it can be seen that during the base case situation, the voltage magnitude at Bus-12 is around 1.05 p.u., whereas with each event the system becomes more stressed and finally collapses, during which the voltage magnitude is 0.657 p.u. From fig. 3.5, it can be seen that initially the voltage angle is -15.07 degrees, and which each event, the angle separation starts increasing such that during the collapse, the angle is as high as -38.36 degrees.

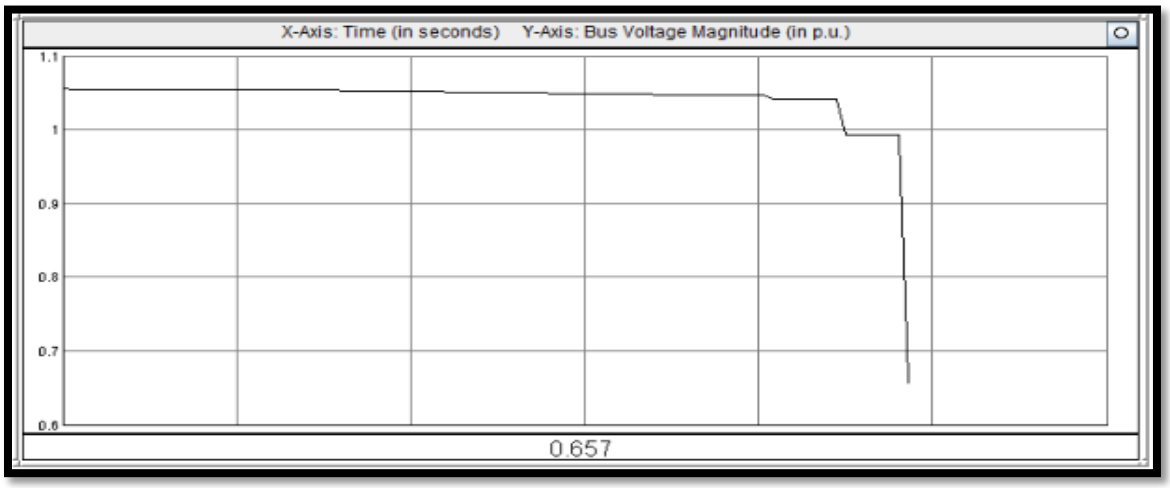

Figure 3.4: RSCAD voltage magnitude changes at Bus-12 for IEEE 14 bus

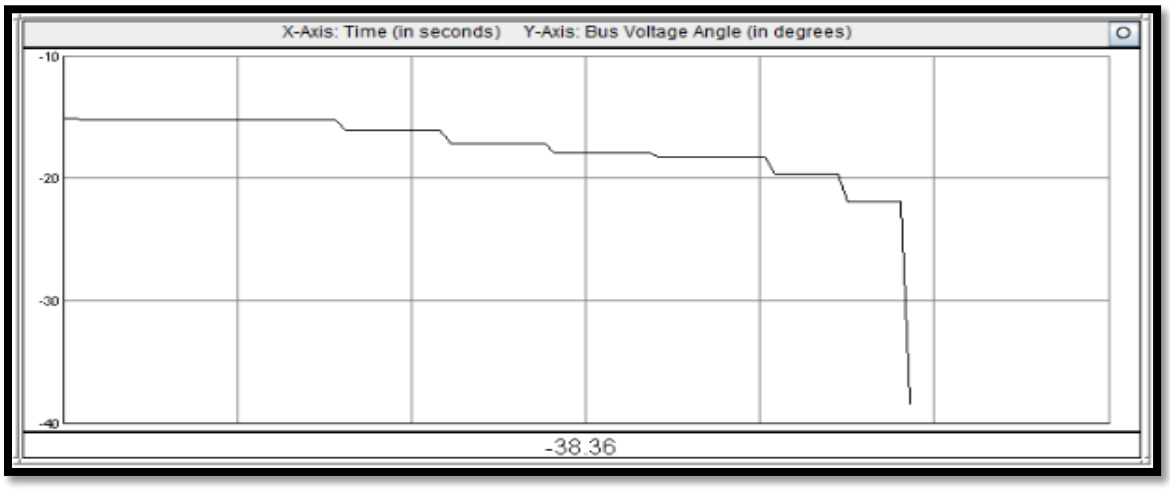

Figure 3.5: RSCAD showing angle changes at Bus-12 for IEEE 14 bus

Figure 3.6 shows a screenshot of the voltage stability visualization application (corresponding to the proposed algorithm) running in the computer at the control center.

It can be seen in fig. 3.6 that at time t = 0 s, when the system is at base case, the VSAI of Bus-12 is 0.3203 (i.e. near "0") signifying a voltage stable scenario. However, when the series of events (as listed in table 3.1) take place over a period of 85 seconds, at t = 85 s, the VSAI shoots up to 1.08023 (i.e. near "1"), clearly indicating a voltage collapse scenario.

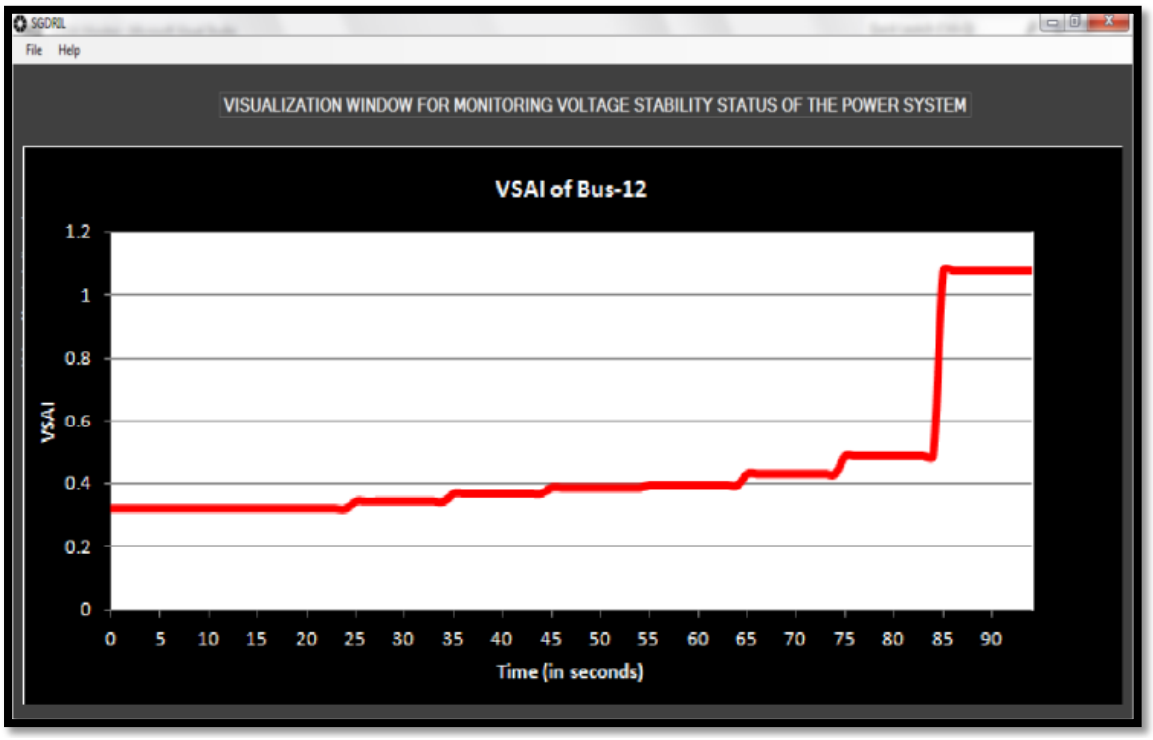

Figure 3.6: VSAI leading to voltage collapse from t = 0 s to t = 85 s

Table 3.2: VSAI in real time for each event leading to voltage collapse

Event No. & Time	VSAI recorded during the Event at Bus-12	Voltage Stability Status
Base Case	0.32030	**Stable**
1 at t=25s	0.34381	**Stable**
2 at t=35s	0.36909	**Stable**
3 at t=45s	0.38773	**Stable**
4 at t=55s	0.39513	**Stable**
5 at t=65s	0.43073	**Stable**
6 at t=75s	0.48802	**Stable**
7 at t=85s	1.08023	**Unstable**

Table 3.3 shows the propagation delays among the monitored bus, slack bus and the control center as simulated in the NS3 software.

Table 3.3: Propagation delays between substations and control center

From Gateway	*To Gateway*	*Propagation delay (in ms)*
Bus 12	Bus 1	1.26955
Bus 12	Control Center	1.46955

3.1.3.2 Simulation of a possible voltage collapse scenario in an IEEE-30 Bus test case using the Real Time Test bed:

The IEEE-30 Bus test case has been modeled in RSCAD, in which Bus-30 has a PMU for real time monitoring of voltage stability.

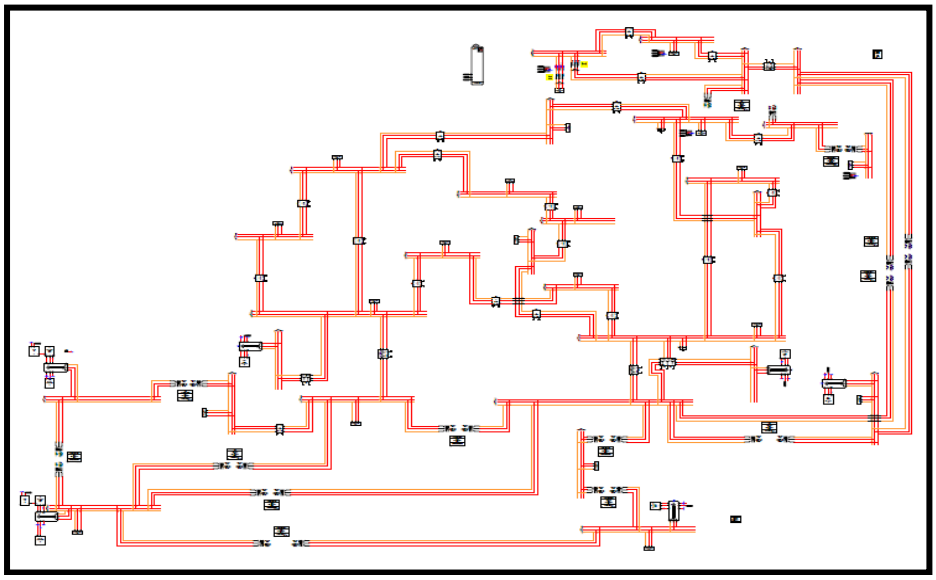

Figure 3.7: IEEE-30 bus test case modeled in RSCAD for real time simulation

Table-3.4 shows the series of events that have been simulated using the RSCAD test case in RTDS for a possible voltage collapse scenario, assuming that initially the system is at base case.

Table 3.4: Series of events leading to voltage collapse in IEEE-30 bus test case

Event No. & Time	***Event Description***
1 at t=35s	Load at Bus-24 increases such that the real power consumption is 25 MW and the reactive power consumption is 19.2 MVAR. (Base Case: 8.61 MW & 6.61 MVAR)
2 at t=50s	Load at Bus-26 increases such that the real power consumption is 15 MW and the reactive power consumption is 9.69 MVAR. (Base Case: 3.51 MW & 2.21 MVAR)
3 at t=65s	Load at Bus-29 increases such that the real power consumption is 7 MW and the reactive power consumption is 2.4 MVAR. (Base Case: 2.31 MW & 0.81 MVAR)
4 at t=80s	Load at Bus-30 increases such that the real power consumption is 30 MW and the reactive power consumption is 5.09 MVAR. (Base Case: 10.51 MW & 1.81 MVAR)
5 at t=95s	Inverse Time Over-current relay (hardware relay) trips the transmission line connecting Bus-27 and Bus-30 due to loading of the line above the set pick up value.

The Event-5 (in the above table) finally leads to a voltage collapse. Figure 3.8 shows the voltage magnitude at the Bus-30 and fig. 3.9 shows the voltage angle at the Bus-30, as simulated in real time in RTDS runtime. From fig. 3.8, it can be seen that during the base case situation, the voltage magnitude at Bus-30 is around 1 p.u., whereas with each event the system becomes more stressed and finally collapses, during which the voltage magnitude is 0.6511 p.u. From fig. 3.9, it can be seen that initially the voltage angle is -17.94 degrees, and which each event, the angle separation starts increasing such that during the collapse, the angle is as high as -40.61 degrees.

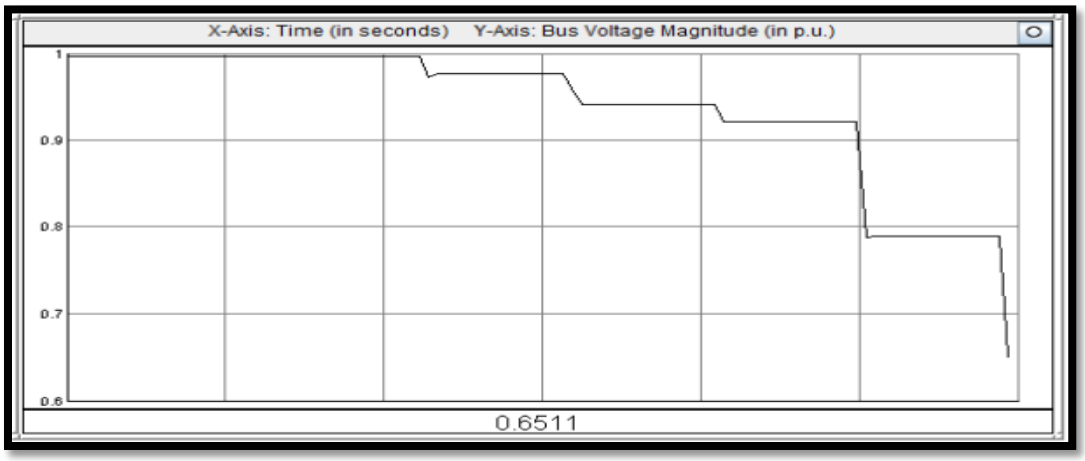

Figure 3.8: RSCAD showing voltage magnitude changes at bus-30 for IEEE 30 bus

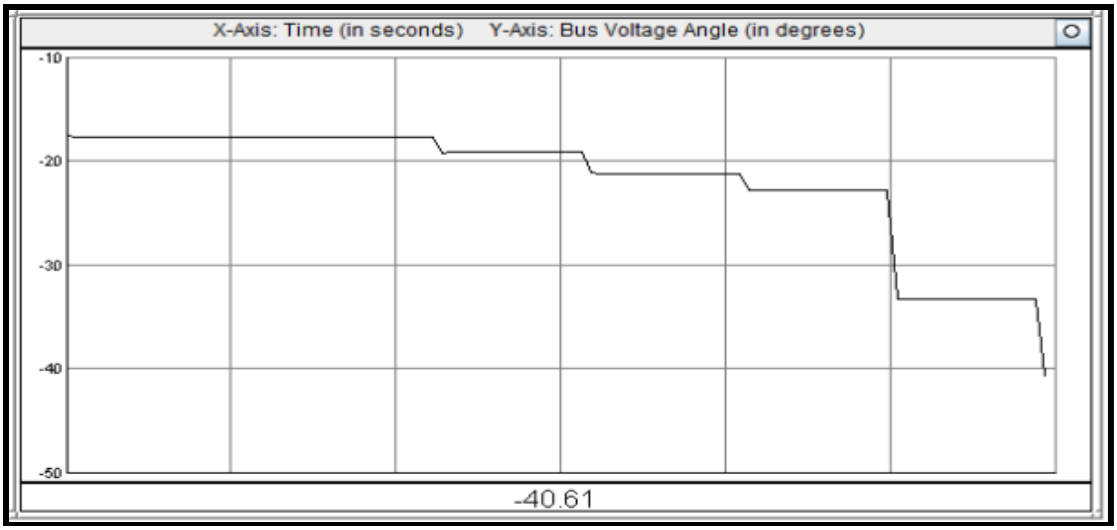

Figure 3.9: RSCAD showing angle changes at bus-30 for IEEE 30 bus

It can be seen in fig. 3.10 that at time t = 0 s, when the system is at base case, the VSAI of Bus-30 is 0.38107 (i.e. near "0") signifying a voltage stable scenario. However, when the series of events (as listed in table 3.4) take place over a period of 95 seconds, at t = 95 s, the VSAI shoots up to 1.09668 (i.e. near "1"), clearly indicating a voltage collapse scenario.

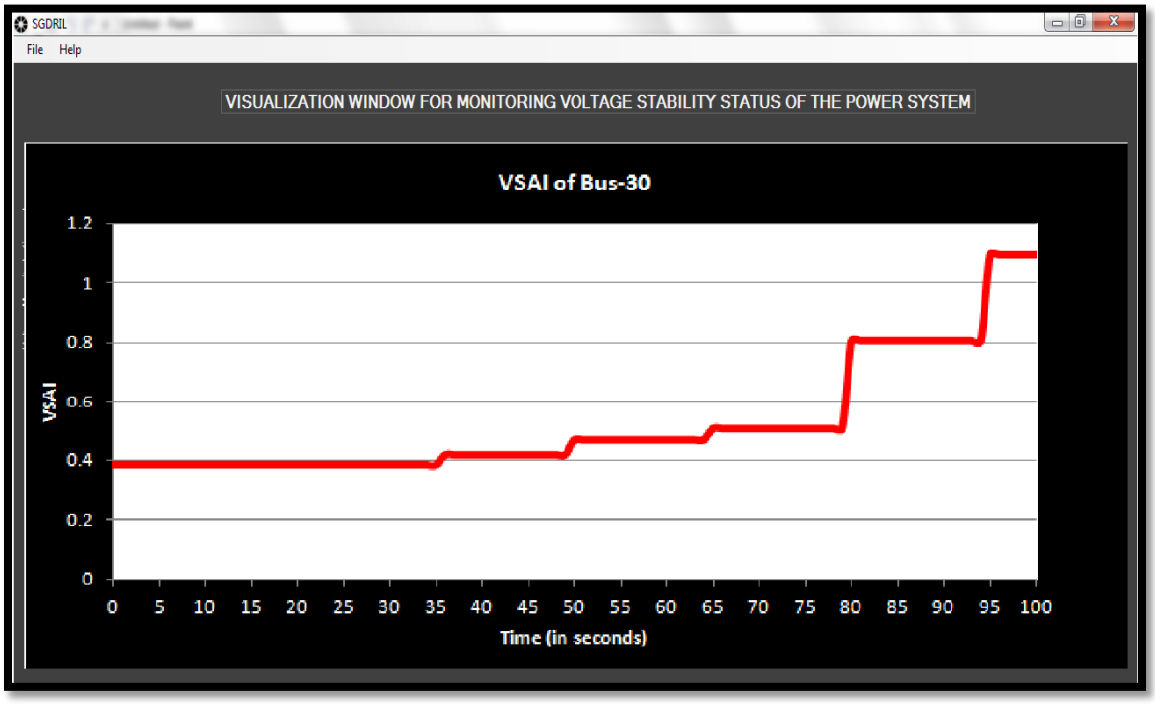

Figure 3.10: VSAI leading to voltage collapse from t = 0 s to t = 95 s

Table 3.5: VSAI computed in real time for each event leading to voltage collapse

Event No. & Time	VSAI recorded during the Event at Bus-30	Voltage Stability Status
Base Case	0.38107	**Stable**
1 at t=35s	0.41658	**Stable**
2 at t=50s	0.46717	**Stable**
3 at t=65s	0.50554	**Stable**
4 at t=80s	0.80496	**Stable**
5 at t=95s	1. 09668	**Unstable**

Table 3.6 shows the propagation delays among the monitored bus, slack bus and the control center as simulated in the NS3 software.

Table 3.6: Propagation delays between substations and control center for 30 bus

From Gateway	***To Gateway***	***Propagation delay (in ms)***
Bus 30	Bus 1	1.85426
Bus 30	Control Center	2.05426

3.1.4 Conclusion from Test Results

Increase in system loading has the potential of causing a small disturbance type voltage instability, whereas contingencies like tripping of transmission lines have the potential of causing large disturbance voltage instability. Both these system conditions have been simulated in real time using the RTDS. From the online results that have been obtained and presented above for different IEEE test cases (i.e. IEEE 14 Bus test case & IEEE 30 bus test case) under different system conditions causing voltage instability problems, it can be seen that the results are in accordance with the static theory of voltage stability analysis [4-5]. The same method of online simulation using the RTDS and the hardware and software devices can be used for validating the accuracy of different online voltage stability algorithms. The voltage stability algorithm has also been implemented using Structured Text language (a type of PLC language) in the Synchrophasor Vector Processor (SVP) instead of the C-language on Linux platform on the automation computer, and exact same results have been obtained.

3.2 Comparing State Estimation Algorithms Using Synchrophasor Data

In performing PMU accuracy evaluation in an absolute sense and under various conditions (such as amplitude and frequency transients, waveform distortion etc.) it is imperative that the output of a PMU under test is compared to the output of a "Standard PMU". Since the existing standards do not presently address this issue, a Standard PMU was designed and implemented using National Instruments data acquisition hardware and custom software. The Standard PMU software was implemented within the WinXFM program. Since the PMU capability was added within the data acquisition system as an object oriented software component we refer to it as a "Virtual PMU".
The standard PMU is used as a benchmark against which the accuracy of the PMU under test is evaluated. Therefore, it is necessary that the standard PMU provides accuracy that exceeds the accuracy required by the standards and remains accurate during typical power system voltage and current amplitude and frequency transients and waveform distortion.

PMU implementations are based on the direct evaluation of the discrete Fourier transform:

$$\vec{V} = \frac{\omega \Delta t}{2\pi}\left(\sum_{k=k_1}^{k_2} a_k \cos(\omega k \Delta t)\, v_k - i \sum_{k=k_1}^{k_2} a_k \sin(\omega k \Delta t)\, v_k\right)$$

where a_k are the waveform samples. The above expression yields the exact phasor of a sampled waveform only if the waveform period is an integer multiple of the sampling rate, so that the summation index range spans an integer number of fundamental frequency periods. (It also assumes that no aliasing has occurred during the sampling, i.e. the original analog waveform does not contain any frequency components higher than half the sampling rate).

Since practical data acquisition systems operate with a fixed sampling rate while the power system frequency varies, in general the waveform period is **not** an integer multiple of the sampling rate. This results in a significant error in the phasor computation. A common approach to reduce this error is to apply low pass filtering on the computed phasors. However, this approach introduces large phasor computation errors during amplitude and frequency transients.

In the standard PMU, this issue is addressed using *fractional sample integration*. This method accurately evaluates the Fourier integral by taking into account the contributions of the fractional end intervals that occur whenever the waveform period is not an integer multiple of the sampling rate. For example, consider the function illustrated in fig. 3.11. A single period of the function to be integrated spans 17.5 sampling intervals. Computing the integral over a single cycle using trapezoidal integration requires the summation of the 17 trapezoid areas located between successive samples plus the area indicated by the yellow trapezoid which spans a fraction of a sampling interval. Using the trapezoidal approximation, this area can be computed from the sampled values

bracketing the sampling interval. This procedure results in a modified expression for the Discrete Fourier transform that takes into account fractional samples:

$$\vec{V} = \frac{\omega \Delta t}{2\pi}\left(\sum_{k=k_1}^{k_2} c_k a_k \cos(\omega k \Delta t)\, v_k - i \sum_{k=k_1}^{k_2} c_k a_k \sin(\omega k \Delta t)\, v_k\right)$$

where c_k are coefficients which depend on the duration of the fractional samples.

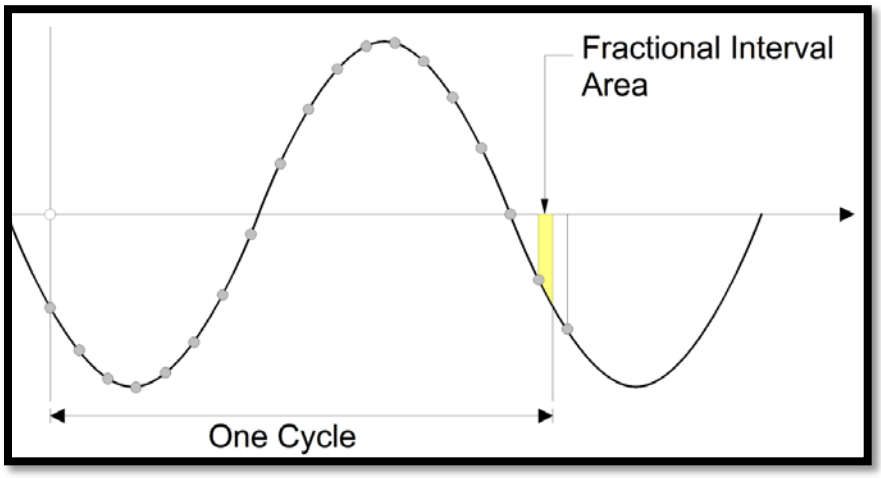

Figure 3.11: Fractional sample integration

The fractional sample integration method can be also implemented using *quadratic integration*. For this purpose, the function to be integrated is approximated with quadratic segments where each segment spans two sampling intervals, as illustrated in fig. 3.12. The resulting expression is similar to the one derived using trapezoidal integration, but with different c_k coefficients.

In order to evaluate the performance of the standard PMU algorithm both trapezoidal and quadratic approaches were implemented and a parametric error analysis was performed. It was found that the trapezoidal fractional integration method substantially reduces the error that occurs with traditional DFT, while the quadratic method performs slightly better than the trapezoidal method for sampling rates above 4 kHz. The results of the parametric analysis are illustrated in fig. 3.13, which shows a plot of the phase angle error of a 60 Hz waveform versus the sampling rate. The plot includes traces for the trapezoidal method (blue trace) and the quadratic method (green trace). It also includes the phase angle error occurring when no fractional sample error correction is performed (red trace).

Table 3.7 summarizes the results for a sampling rate of 8 kHz. As it can be seen the estimation of frequency and phasors with the standard PMU is highly accurate. The

standard PMU is used for testing the performance of various commercially available PMUs as well as for various applications, such as distributed state estimation, stability monitoring, etc.

Table 3.7: Phase error at sampling rate of 8 KHz

Correction Method	Phase Error (Degrees)
None	0.2
Trapezoidal	0.00004
Quadratic	0.00002

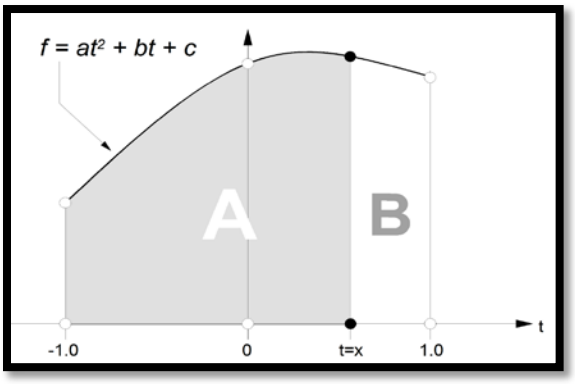

Figure 3.12: Quadratic approximation of a function from three successive samples

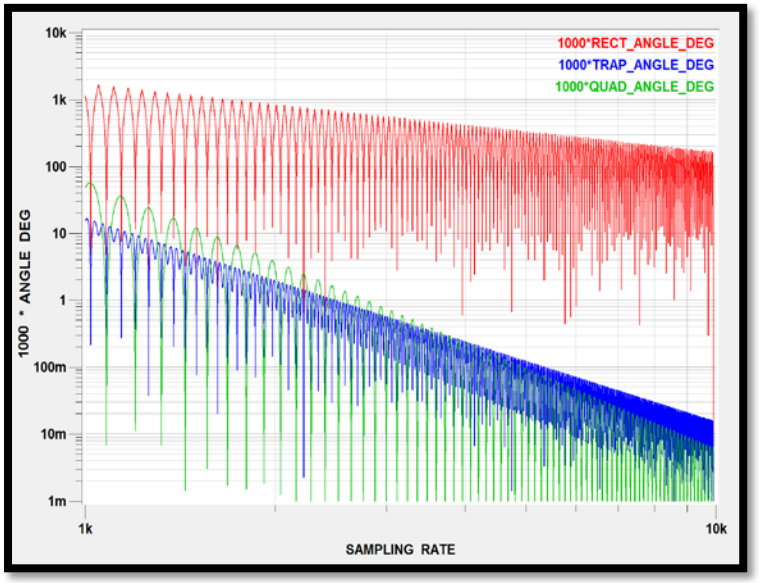

Figure 3.13: Standard PMU algorithm performance

3.3 Dynamic State Estimation Based Protection Algorithms for Transformers

In this section, a new transformer protection approach based on dynamic state estimation and PMU synchronized data has been developed and tested (setting-less protection). The transformer models used, as well as the implementation issues of the method are discussed.

3.3.1 Description of the approach

The architecture of the setting-less protection relay for a transformer is shown in fig. 3.14. The relay requires the model of the transformer as well as the model of the measurements (data acquisition system). The measurements may consist of actual measurements as well as derived, virtual and pseudo measurements. The transformer model must be cast in a standard quadratic form, referred to as Algebraic Quadratic Companion Form (AQCF), which is defined in this document. Given the pointers that connect the measured quantities to state variables of the transformer model, the model (equations) for the actual, virtual and pseudo-measurements are automatically obtained. Given the state equations and a model that links states to measurements, a dynamic state estimation is continuously executed by the protection relay, and from it the results regarding protection decision (trip/no trip) as well bad data detection and identification can be obtained. .

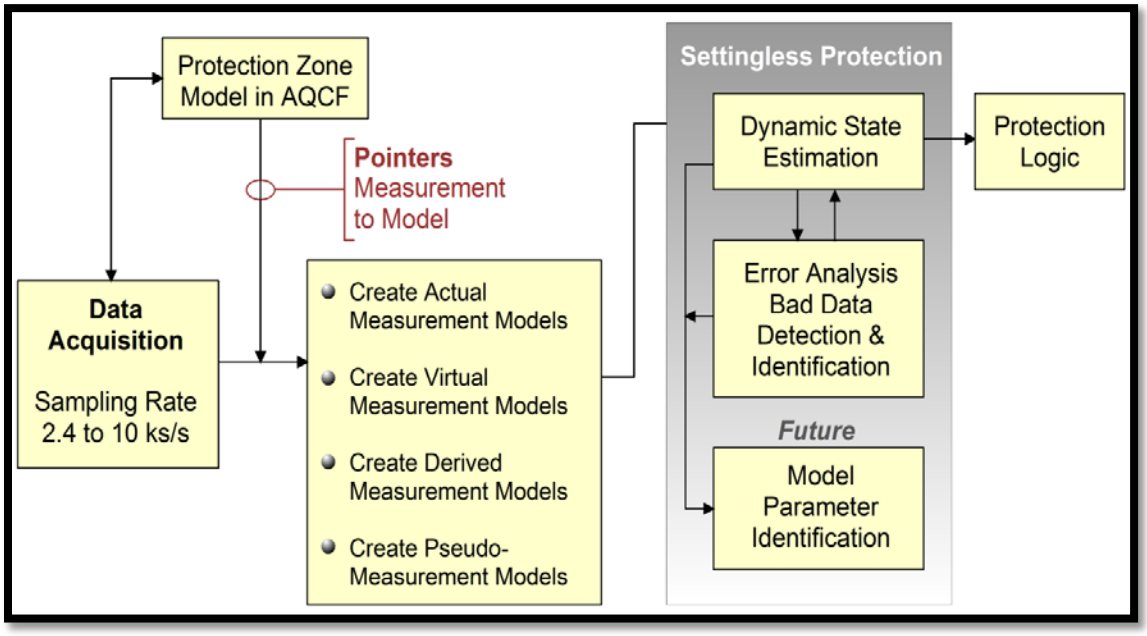

Figure 3.14: Architecture of the dynamic state estimation based protective relay

In this approach, the time-domain component model used is in AQCF. The AQCF is obtained from the model of the transformer described in terms of a set of linear and nonlinear algebraic and differential equations with the following procedure: first the model is quadratized with the introduction of additional state variables resulting in a set

of linear and quadratic algebraic and differential equations. Subsequently the quadratized model is integrated with the quadratic integration method yielding the model in the form of a set of Algebraic Quadratic Companion Form (AQCF). As a result of the quadratic integration, the state equations are written in terms of the state of the component at two consecutive time steps (namely t and t_m) and past history values. Hence, as shown in fig. 3.15, the dynamic state estimation algorithm that enables setting-less protection operates on measurements (z) of two consecutive time instances t and $t_m = t\text{-}t_s$ (note that t_s signifies the sampling period). For a sampling rate of 5000 samples per second, it is implied that t_s is 200μs, which in turn implies that the analytics of the setting-less protection algorithm must be performed (as two sets of new measurements arrive) within an interval of 400μs, before the next set of data arrives. As a goal for this project, an execution time of 200μs has been targeted. The overall approach is illustrated in fig. 3.16.

The details of this approach as applied to the protection of a transformer is discussed next.

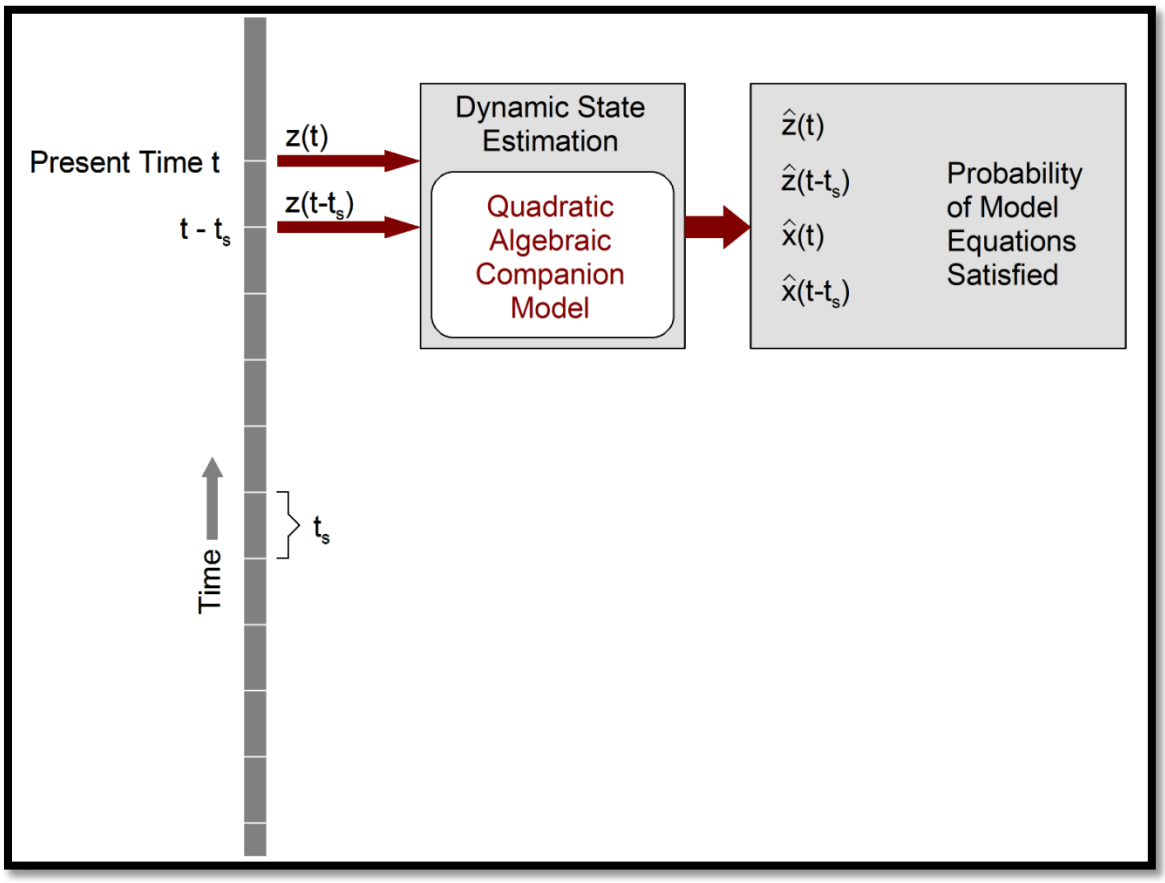

Figure 3.15: Illustration of time samples for iteration of the setting-less relay

3.3.2 Transformer Setting-less Protection Approach Description

3.3.2.1 Transformer Model

A detailed transformer model has been derived in time domain and has been cast in AQCF using quadratic integration. Here we present the final AQCF model of the three-phase, two-winding, variable-tap, and saturable-core transformer as follows:

$$\begin{bmatrix} i_{3\phi}(t) \\ 0 \\ i_{3\phi}(t_m) \\ 0 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \cdot \begin{bmatrix} v_{3\phi}(t) \\ y_{3\phi}(t) \\ v_{3\phi}(t_m) \\ y_{3\phi}(t_m) \end{bmatrix} - \begin{bmatrix} N_{11} & N_{12} \\ N_{21} & N_{22} \\ N_{31} & N_{32} \\ N_{41} & N_{42} \end{bmatrix} \cdot \begin{bmatrix} v_{3\phi}(t-h) \\ y_{3\phi}(t-h) \end{bmatrix} + \begin{bmatrix} f_{3\phi,1}(t) \\ f_{3\phi,2}(t) \\ f_{3\phi,1}(t_m) \\ f_{3\phi,2}(t_m) \end{bmatrix} \tag{3.1}$$

where:

$$i_{3\phi}(t) = [i_a(t), i_b(t), i_c(t), i_A(t), i_B(t), i_C(t), i_N(t)]^T \tag{3.2}$$

$$Y_{eq} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \tag{3.3}$$

$$v_{3\phi}(t) = [v_a(t), v_b(t), v_c(t), v_A(t), v_B(t), v_C(t), v_N(t)]^T \tag{3.4}$$

$$\begin{aligned} y_{3\phi}(t) = [&i_{mA}(t), e_A(t), \lambda_A(t), i_{1LA}(t), i_{3LA}(t), y_{1A}(t), y_{2A}(t), y_{3A}(t), z_A(t), \\ &i_{mB}(t), e_B(t), \lambda_B(t), i_{1LB}(t), i_{3LB}(t), y_{1B}(t), y_{2B}(t), y_{3B}(t), z_B(t), \\ &i_{mC}(t), e_C(t), \lambda_C(t), i_{1LC}(t), i_{3LC}(t), y_{1C}(t), y_{2C}(t), y_{3C}(t), z_C(t)]^T \end{aligned} \tag{3.5}$$

$$N_{eq} = \begin{bmatrix} N_{11} & N_{12} \\ N_{21} & N_{22} \\ N_{31} & N_{32} \\ N_{41} & N_{42} \end{bmatrix} \tag{3.6}$$

$$f_{3\phi,1}(t) = \begin{bmatrix} x_{1\phi}(t)^T \cdot Q_1 \cdot x_{1\phi}(t) \\ x_{1\phi}(t)^T \cdot Q_2 \cdot x_{1\phi}(t) \\ \vdots \\ x_{1\phi}(t)^T \cdot Q_7 \cdot x_{1\phi}(t) \end{bmatrix} \tag{3.7}$$

$$f_{3\phi,2}(t) = \begin{bmatrix} x_{1\phi}(t)^T \cdot Q_8 \cdot x_{1\phi}(t) \\ x_{1\phi}(t)^T \cdot Q_9 \cdot x_{1\phi}(t) \\ \vdots \\ x_{1\phi}(t)^T \cdot Q_{27} \cdot x_{1\phi}(t) \end{bmatrix} \tag{3.8}$$

The detailed derivation of this model is not shown here in the interest of space.
The state variables for a three-phase, delta-wye transformer (n = 5) are 68 (34 for time step t and 34 for intermediate time step t_m), as listed in Table 3.8.

Table 3.8: All state variables of the three-phase transformer (n = 5)

State	Type	Time	Description
$x_1 = v_a(t)$	External	t	Phase-a terminal voltage at the primary side
$x_2 = v_b(t)$	External	t	Phase-b terminal voltage at the primary side
$x_3 = v_c(t)$	External	t	Phase-c terminal voltage at the primary side
$x_4 = v_A(t)$	External	t	Phase-A terminal voltage at the secondary side
$x_5 = v_B(t)$	External	t	Phase-B terminal voltage at the secondary side
$x_6 = v_C(t)$	External	t	Phase-C terminal voltage at the secondary side
$x_7 = v_N(t)$	External	t	Neutral terminal voltage at the secondary side
$x_8 = i_{mA}(t)$	Internal	t	Magnetizing current at the primary-side, phase-a coil
$x_9 = e_A(t)$	Internal	t	Phase-a winding voltage at the primary side
$x_{10} = \lambda_A(t)$	Internal	t	Magnetic flux linkage at the phase-a core
$x_{11} = i_{1LA}(t)$	Internal	t	Phase-a terminal current at the primary side
$x_{12} = i_{3LA}(t)$	Internal	t	Phase-A terminal current at the secondary side
$x_{13} = y_{1A}(t)$	Internal	t	Additional state for the nonlinear term at phase a
$x_{14} = y_{2A}(t)$	Internal	t	Additional state for the nonlinear term at phase a
$x_{15} = y_{3A}(t)$	Internal	t	Additional state for the nonlinear term at phase a
$x_{16} = z_A(t)$	Internal	t	Additional state for the nonlinear term at phase a
$x_{17} = i_{mB}(t)$	Internal	t	Magnetizing current at the primary-side, phase-b coil
$x_{18} = e_B(t)$	Internal	t	Phase-b winding voltage at the primary side
$x_{19} = \lambda_B(t)$	Internal	t	Magnetic flux linkage at the phase-b core
$x_{20} = i_{1LB}(t)$	Internal	t	Phase-b terminal current at the primary side
$x_{21} = i_{3LB}(t)$	Internal	t	Phase-B terminal current at the secondary side
$x_{22} = y_{1B}(t)$	Internal	t	Additional state for the nonlinear term at phase b
$x_{23} = y_{2B}(t)$	Internal	t	Additional state for the nonlinear term at phase b
$x_{24} = y_{3B}(t)$	Internal	t	Additional state for the nonlinear term at phase b
$x_{25} = z_B(t)$	Internal	t	Additional state for the nonlinear term at phase b

Table 3.8 continued

State	Type	Time	Description
$x_{26} = i_{mC}(t)$	Internal	t	Magnetizing current at the primary-side, phase-c coil
$x_{27} = e_C(t)$	Internal	t	Phase-c winding voltage at the primary side
$x_{28} = \lambda_C(t)$	Internal	t	Magnetic flux linkage at the phase-c core
$x_{29} = i_{1LC}(t)$	Internal	t	Phase-c terminal current at the primary side
$x_{30} = i_{3LC}(t)$	Internal	t	Phase-C terminal current at the secondary side
$x_{31} = y_{1C}(t)$	Internal	t	Additional state for the nonlinear term at phase c
$x_{32} = y_{2C}(t)$	Internal	t	Additional state for the nonlinear term at phase c
$x_{33} = y_{3C}(t)$	Internal	t	Additional state for the nonlinear term at phase c
$x_{34} = z_C(t)$	Internal	t	Additional state for the nonlinear term at phase c
$x_{35} = v_a(t_m)$	External	t_m	Phase-a terminal voltage at the primary side
$x_{36} = v_b(t_m)$	External	t_m	Phase-b terminal voltage at the primary side
$x_{37} = v_c(t_m)$	External	t_m	Phase-c terminal voltage at the primary side
$x_{38} = v_A(t_m)$	External	t_m	Phase-A terminal voltage at the secondary side
$x_{39} = v_B(t_m)$	External	t_m	Phase-B terminal voltage at the secondary side
$x_{40} = v_C(t_m)$	External	t_m	Phase-C terminal voltage at the secondary side
$x_{41} = v_N(t_m)$	External	t_m	Neutral terminal voltage at the secondary side
$x_{42} = i_{mA}(t_m)$	Internal	t_m	Magnetizing current at the primary-side, phase-a coil
$x_{43} = e_A(t_m)$	Internal	t_m	Phase-a winding voltage at the primary side
$x_{44} = \lambda_A(t_m)$	Internal	t_m	Magnetic flux linkage at the phase-a core
$x_{45} = i_{1LA}(t_m)$	Internal	t_m	Phase-a terminal current at the primary side
$x_{46} = i_{3LA}(t_m)$	Internal	t_m	Phase-A terminal current at the secondary side
$x_{47} = y_{1A}(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase a
$x_{48} = y_{2A}(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase a
$x_{49} = y_{3A}(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase a
$x_{50} = z_A(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase a
$x_{51} = i_{mB}(t_m)$	Internal	t_m	Magnetizing current at the primary-side, phase-b coil

Table 3.8 continued

State	Type	Time	Description
$x_{52} = e_B(t_m)$	Internal	t_m	Phase-b winding voltage at the primary side
$x_{53} = \lambda_B(t_m)$	Internal	t_m	Magnetic flux linkage at the phase-b core
$x_{54} = i_{1LB}(t_m)$	Internal	t_m	Phase-b terminal current at the primary side
$x_{55} = i_{3LB}(t_m)$	Internal	t_m	Phase-B terminal current at the secondary side
$x_{56} = y_{1B}(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase b
$x_{57} = y_{2B}(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase b
$x_{58} = y_{3B}(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase b
$x_{59} = z_B(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase b
$x_{60} = i_{mC}(t_m)$	Internal	t_m	Magnetizing current at the primary-side, phase-c coil
$x_{61} = e_C(t_m)$	Internal	t_m	Phase-c winding voltage at the primary side
$x_{62} = \lambda_C(t_m)$	Internal	t_m	Magnetic flux linkage at the phase-c core
$x_{63} = i_{1LC}(t_m)$	Internal	t_m	Phase-c terminal current at the primary side
$x_{64} = i_{3LC}(t_m)$	Internal	t_m	Phase-C terminal current at the secondary side
$x_{65} = y_{1C}(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase c
$x_{66} = y_{2C}(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase c
$x_{67} = y_{3C}(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase c
$x_{68} = z_C(t_m)$	Internal	t_m	Additional state for the nonlinear term at phase c

To implement the setting-less transformer protection for a three-phase delta/wye connected transformer, the following measurements are defined:

Actual measurements

- six voltages at time t (phase a-N, phase b-N, phase c-N, phase A-N, phase B-N, and phase C-N)
- seven currents at time t (phase a, phase b, phase c, phase A, phase B, phase C, and phase N)
- six voltages at time t_m (phase a-N, phase b-N, phase c-N, phase A-N, phase B-N, and phase C-N)
- seven currents at time t_m (phase phase a, phase b, phase c, phase A, phase B, phase C, and phase N).

These measurements have a measurement error depended upon the accuracy of the meters used. We represent this error with its standard deviation.

Virtual measurements

These include measurements with a value equal to zero at time t [8th- to 34th-row in equation (3.1) and measurements with a value equal to zero at time t_m (42th- to 68th-row in equation (3.2). These measurements represent the zero value on the left hand side of the 8th- to 34th-row and 42nd- to 68th-row in equation (3.2). The virtual measurements are known with absolute precision and normally we should assign a measurement error of zero. However the algorithm will suffer a singularity if an error of zero is used. For this reason we use a standard deviation which is equal to 0.001pu.

Table 3.9: Actual across measurements for the three-phase transformer

Type	Name	Measurement Model	Standard Deviation
Across	voltage_aN	$z_1 = v_a(t) - v_N(t)$	0.01 (p.u.) * Vscaleh
Across	voltage_bN	$z_2 = v_b(t) - v_N(t)$	0.01 (p.u.) * Vscaleh
Across	voltage_cN	$z_3 = v_c(t) - v_N(t)$	0.01 (p.u.) * Vscaleh
Across	voltage_AN	$z_4 = v_A(t) - v_N(t)$	0.01 (p.u.) * Vscalel
Across	voltage_BN	$z_5 = v_B(t) - v_N(t)$	0.01 (p.u.) * Vscalel
Across	voltage_CN	$z_6 = v_C(t) - v_N(t)$	0.01 (p.u.) * Vscalel
Across	voltage_aNm	$z_7 = v_a(t_m) - v_N(t_m)$	0.01 (p.u.) * Vscaleh
Across	voltage_bNm	$z_8 = v_b(t_m) - v_N(t_m)$	0.01 (p.u.) * Vscaleh
Across	voltage_cNm	$z_9 = v_c(t_m) - v_N(t_m)$	0.01 (p.u.) * Vscaleh
Across	voltage_ANm	$z_{10} = v_A(t_m) - v_N(t_m)$	0.01 (p.u.) * Vscalel
Across	voltage_BNm	$z_{11} = v_B(t_m) - v_N(t_m)$	0.01 (p.u.) * Vscalel
Across	voltage_CNm	$z_{12} = v_C(t_m) - v_N(t_m)$	0.01 (p.u.) * Vscalel

Pseudo measurements

These measurements represent quantities that are normally not measured, such as ground voltage and current in the neutral. Typically, it is assumed that these measurements have a relatively large measurement error with standard deviation equal to 0.1pu. For this transformer we define the following pseudo-measurements: one voltage at time t (phase N-g) and one voltage at time t_m (phase N-g).

Note that for this three-phase transformer, there are 26 actual measurements, 54 virtual measurements, and 2 pseudo measurements; there are a total of 82 measurements. It is noted that there are 68 states, and therefore, this provides a redundancy of 20.6% (i.e., (82-68)/68).

All across, through, virtual, and pseudo measurements that are used for the dynamic state estimator are listed in Table 3.9, Table 3.10, Table 3.11, and Table 3.12, respectively. The standard deviations are given in % in a per-unit system that uses the transformer rated values as bases. It is important to point out that when two consecutive sampling points are imported, the first point becomes a measurement for the intermediate time t_m, and the second point becomes a measurement for the current time t.

Table 3.10: Actual through measurements for the three-phase transformer

Type	Name	Measurement Model	Standard Deviation
Through	current_a	$z_1 = i_a(t)$ = *1st-row in eq.* (3.1)	0.01 (p.u.) * Iscaleh
Through	current_b	$z_2 = i_b(t)$ = *2nd-row in eq.* (3.1)	0.01 (p.u.) * Iscaleh
Through	current_c	$z_3 = i_c(t)$ = *3rd-row in eq.* (3.1)	0.01 (p.u.) * Iscaleh
Through	current_A	$z_4 = i_A(t)$ = *4th-row in eq.* (3.1)	0.01 (p.u.) * Iscalel
Through	current_B	$z_5 = i_B(t)$ = *5th-row in eq.* (3.1)	0.01 (p.u.) * Iscalel
Through	current_C	$z_6 = i_C(t)$ = *6th-row in eq.* (3.1)	0.01 (p.u.) * Iscalel
Through	current_N	$z_7 = i_N(t)$ = *7th-row in eq.* (3.1)	0.01 (p.u.) * Iscalel
Through	current_am	$z_8 = i_a(t_m)$ = *35th-row in eq.* (3.1)	0.01 (p.u.) * Iscaleh
Through	current_bm	$z_9 = i_b(t_m)$ = *36th-row in eq.* (3.1)	0.01 (p.u.) * Iscaleh
Through	current_cm	$z_{10} = i_c(t_m)$ = *37th-row in eq.* (3.1)	0.01 (p.u.) * Iscaleh
Through	current_Am	$z_{11} = i_A(t_m)$ = *38th-row in eq.* (3.1)	0.01 (p.u.) * Iscalel
Through	current_Bm	$z_{12} = i_B(t_m)$ = *39th-row in eq.* (3.1)	0.01 (p.u.) * Iscalel
Through	current_Cm	$z_{13} = i_C(t_m)$ = *40th-row in eq.* (3.1)	0.01 (p.u.) * Iscalel
Through	current_Nm	$z_{14} = i_N(t_m)$ =*41st-row in eq.* (3.1)	0.01 (p.u.) * Iscalel

Table 3.11: Virtual measurements for the three-phase transformer

Type	Name	Measurement Model	Standard Deviation
Virtual	virtual_t_1	$z_1 = 0$ = *8th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_2	$z_2 = 0$ = *9th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_3	$z_3 = 0$ = *10th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_4	$z_4 = 0$ = *11th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_5	$z_5 = 0$ = *12th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_6	$z_6 = 0$ = *13th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_7	$z_7 = 0$ = *14th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_8	$z_8 = 0$ = *15th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_9	$z_9 = 0$ = *16th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_10	$z_{10} = 0$ = *17th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_11	$z_{11} = 0$ = *18th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_12	$z_{12} = 0$ = *19th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_13	$z_{13} = 0$ = *20th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_14	$z_{14} = 0$ = *21st-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_15	$z_{15} = 0$ = *22nd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_16	$z_{16} = 0$ = *23rd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_17	$z_{17} = 0$ = *24th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_18	$z_{18} = 0$ = *25th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_19	$z_{19} = 0$ = *26st-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_20	$z_{20} = 0$ = *27nd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_21	$z_{21} = 0$ = *28rd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_22	$z_{22} = 0$ = *29th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_23	$z_{23} = 0$ = *30th-row in eq.* (3.1)	0.001 (p.u.)

Table 3.11 continued

Type	Name	Measurement Model	Standard Deviation
Virtual	virtual_t_24	$z_{24} = 0$ = *31st-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_25	$z_{25} = 0$ = *32nd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_26	$z_{26} = 0$ = *33rd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_t_27	$z_{27} = 0$ = *34th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_1	$z_{28} = 0$ = *42nd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_2	$z_{29} = 0$ = *43rd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_3	$z_{30} = 0$ = *44th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_4	$z_{31} = 0$ = *45th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_5	$z_{32} = 0$ = *46th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_6	$z_{33} = 0$ = *47th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_7	$z_{34} = 0$ = *48th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_8	$z_{35} = 0$ = *49th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_9	$z_{36} = 0$ = *50th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_10	$z_{37} = 0$ = *51st-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_11	$z_{38} = 0$ = *52nd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_12	$z_{39} = 0$ = *53rd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_13	$z_{40} = 0$ = *54th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_14	$z_{41} = 0$ = *55th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_15	$z_{42} = 0$ = *56th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_16	$z_{43} = 0$ = *57th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_17	$z_{44} = 0$ = *58th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_18	$z_{45} = 0$ = *59th-row in eq.* (3.1)	0.001 (p.u.)

Table 3.11 continued

Type	Name	Measurement Model	Standard Deviation
Virtual	virtual_tm_19	$z_{46} = 0$ = *60th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_20	$z_{47} = 0$ = *61st-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_21	$z_{48} = 0$ = *62nd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_22	$z_{49} = 0$ = *63rd-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_23	$z_{50} = 0$ = *64th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_24	$z_{51} = 0$ = *65th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_25	$z_{52} = 0$ = *66th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_26	$z_{53} = 0$ = *67th-row in eq.* (3.1)	0.001 (p.u.)
Virtual	virtual_tm_27	$z_{54} = 0$ = *68th-row in eq.* (3.1)	0.001 (p.u.)

Table 3.12: Pseudo measurements for the three-phase transformer

Type	Name	Measurement Model	Standard Deviation
Pseudo	voltage_N	$z_1 = 0 = v_N(t)$	0.1 (p.u.) * Vscalel
Pseudo	voltage_Nm	$z_2 = 0 = v_N(t_m)$	0.1 (p.u.) * Vscalel

Note that if there is no actual through measurement for the neutral phase (i.e., phase N), pseudo measurements for the phase-N current can be added with a standard deviation of 0.1 per unit.

The proposed protection algorithm uses four types of measurements: across measurements, through measurements, virtual measurements, and pseudo measurements. It is important to point out that all measurements (e.g., z_1, z_2, ⋯, z_m) can be expressed with the functions of state variables [e.g., $h_1(x)$, $h_2(x)$, ⋯, $h_m(x)$] and measurement errors (e.g., η_1, η_2, ⋯, η_m), forming the following measurement model:

$$z = h(x) + \eta \tag{3.9}$$

where:

$$z = \begin{bmatrix} z_1 \\ z_2 \\ \vdots \\ z_m \end{bmatrix} \tag{3.10}$$

$$h(x) = \begin{bmatrix} h_1(x) \\ h_2(x) \\ \vdots \\ h_m(x) \end{bmatrix} \tag{3.11}$$

$$\eta(x) = \begin{bmatrix} \eta_1(x) \\ \eta_2(x) \\ \vdots \\ \eta_m(x) \end{bmatrix} \tag{3.12}$$

Using the AQCF model of the transformer the measurement model is expressed in the following standard form:

$$z_m = c + \sum_i a_i x_i + \sum_j \sum_k b_{jk} x_j x_k + \eta_m \tag{3.13}$$

where z_m is the measured value, c is the constant term, a_i are the linear coefficient terms, b_{jk} are the nonlinear coefficient terms (i.e., quadratic terms), x_i, x_j, and x_k are the state variables, i, j, and k are the indices of summation, and η_m is the measurement error.

3.3.2.2 Dynamic State Estimation

The dynamic state estimation is obtained using a standard weighted least squares approach, which is relatively straight forward, once the state equations and measurement models have been obtained. A detailed outlined of the method is given in fig. 3.16. Dynamic state estimation is inspired by distributed state estimation work done earlier [11-12].

3.3.3 Protection Logic

The entire protection logic is based on the results of the dynamic state estimator. Once the microprocessor gets the measurements from both sides of a transformer under protection, the dynamic state estimation runs using the transformer AQCF model. Then, the chi-square test is performed to provide the probability that all the actual values for measurements fit to the transformer model. The results of the chi square are used to compute the confidence level that measurements fit the transformer model and therefore the transformer is in a healthy status. If the confidence level drops to a low value for several cycles, then the measurements do not fit the model, thus the internal transformer model is incorrect, indicating an internal fault. As a result, the relay would activate breakers and trip the transformer immediately.

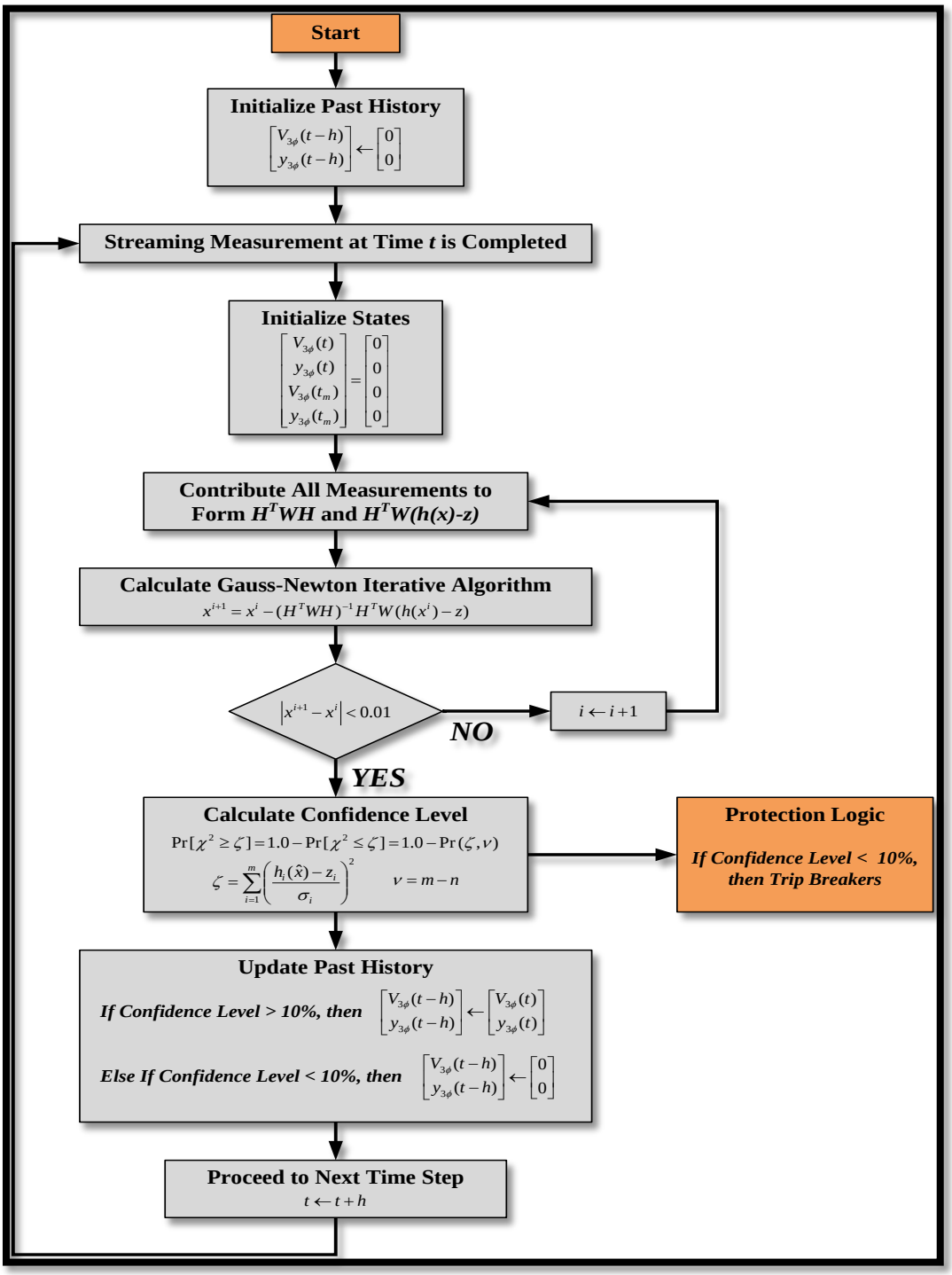

Figure 3.16: Overall algorithm of state estimation

Meanwhile, during the state estimation process, the operating limit is being monitored so that the transformer will be tripped once it violates the operating limit.

The above described transformer protection requires no setting. Time synchronization is quite important for the proposed protection scheme since the algorithm requires synchronized measurements. Therefore the application of this algorithm requires the use of PMUs are equivalent.

3.3.4 Transformer Setting-less protection results

The above described setting-less relay for transformers have been tested with simulated data. Specifically a test system was used to create a number of scenarios. For each scenario the system was simulated and the measurements of the relay were stored in a COMTRADE file.

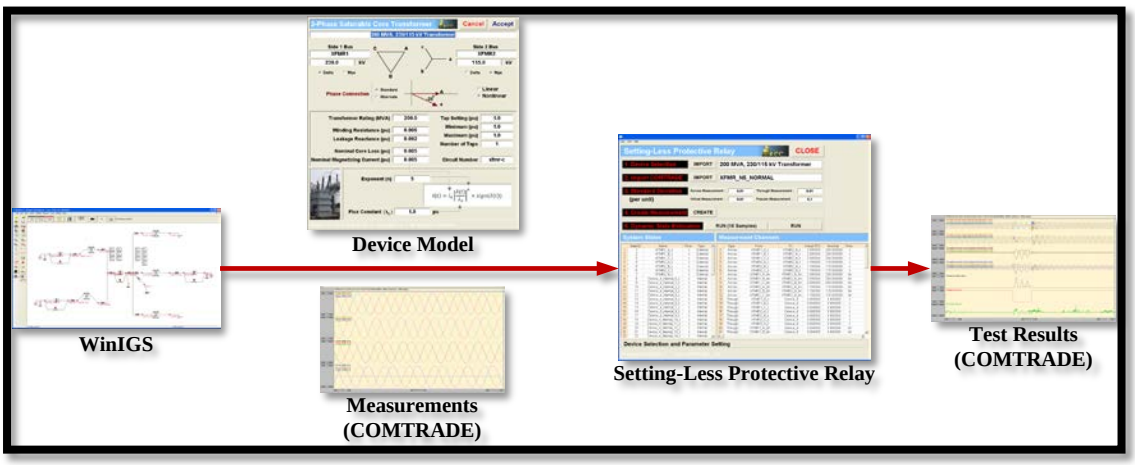

Figure 3.17: Test scheme for verifying the proposed protection method

The simulation was performed with the program WinIGS-T. Both measurements and device model constitute the input data to the setting-less protective relay which in turn performs dynamic state estimation and the protection logic. The protective relay outputs include estimated states, estimated measurements, raw measurements, residuals between estimated and measured values, normalized residuals, and the processing time; these results are also stored in COMTRADE format for additional analysis and performance evaluation of the algorithm. Figure 3.17 describes the overall approach for the feasibility test of the setting-less protection algorithm.

The test system used for numerical tests is shown in fig. 3.18. The system consists of a 15kV-150MVA-rated generator, an 18kV-350MVA-rated generator, a 15kV-200MVA-rated generator, transformers, and transmission lines that connect load on each line. The three-phase transformer under protection is located at the middle of the entire system (see the red circle in fig. 3.18). Monitored are ten voltages and seven currents at both the terminals of the transformer.

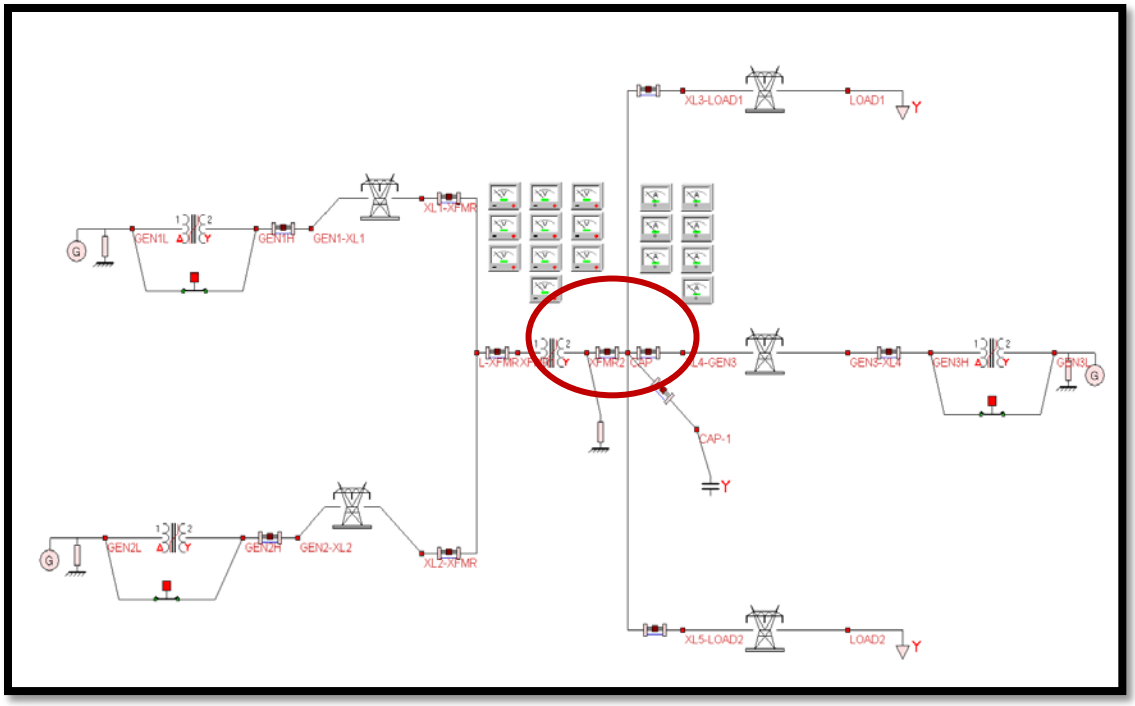

Figure 3.18: Test system for the setting-less protection

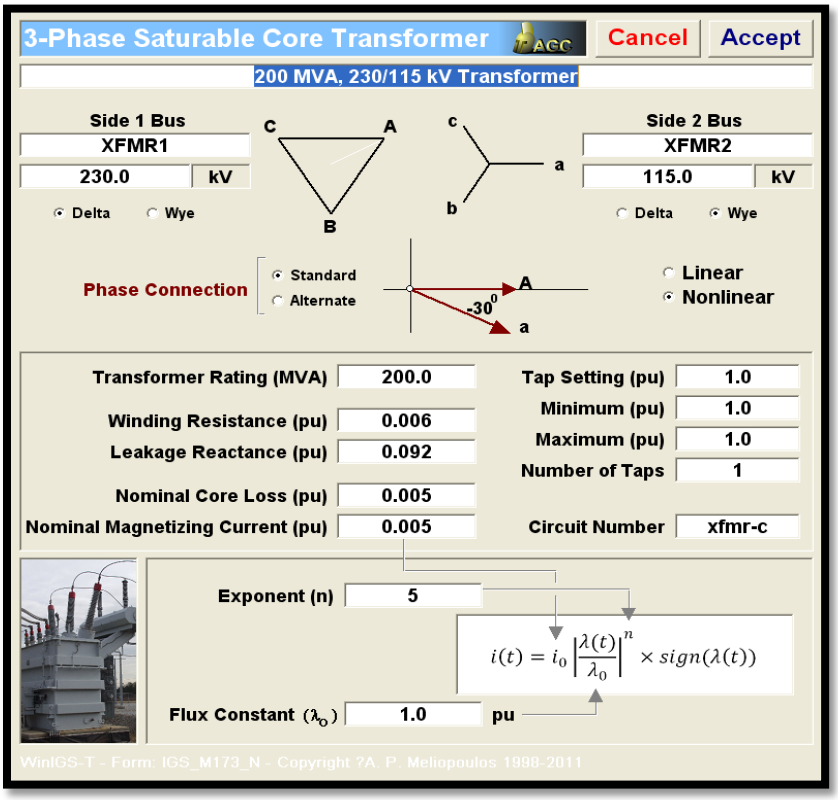

Figure 3.19: Settings of the three-phase transformer under protection

The red area is the transformer zone being protected. As shown in the diagram, the measurements of voltages and currents on both sides are provided by PTs and CTs.

In this test, the exponent *n*, which expresses nonlinear characteristics between the magnetizing current and the flux linkage of the transformer core, is five, and the transformer is delta-wye-connected. The settings of the transformer under protection are shown in fig. 3.19.

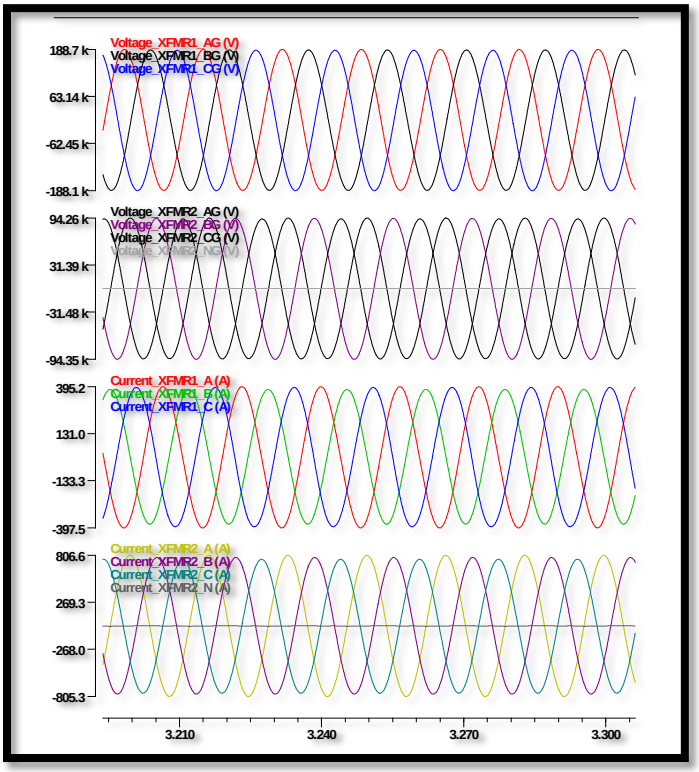

Figure 3.20: Measurement signals of the transformer (Test A: normal operation)

The actual parameters of the single-phase transformer model are given in Table 3.13 (the parameters are identical to all phases of the transformer.)

Table 3.13: Transformer parameters (identical at all phases)

Parameter	Value	Parameter	Value
r_1	2.3805 Ω	r_c	158700 Ω
L_1	0.096822 H	L_m	420.964824 H
r_2	0.198375 Ω	i_0	0.002050
L_2	0.008068 H	λ_0	0.862803
N	0.288675		

Five sets of different measurement signals are illustrated and tested using the setting-less protection scheme:

- Test A: Normal operating condition
- Test B: Transformer energization (inrush current)
- Test C: Transformer overexcitation
- Test D: Through fault condition
- Test E: Internal fault condition

Test A: Normal Operating Condition

The test signals used in this case are shown in fig. 3.20.

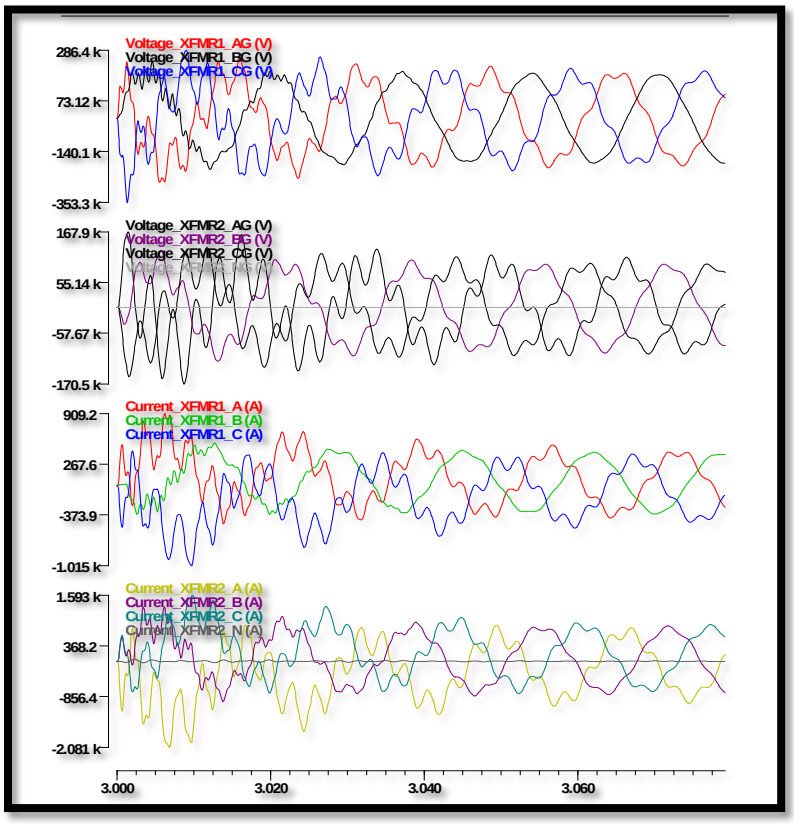

Figure 3.21: Measurement signals of the transformer (Test B: energization)

Test B: Transformer Energization (Inrush Current)

For transformer energization, the test system in fig. 3.18 is used. A set of measurement signals monitored during the energization is shown in the fig. 3.21.

Test C: Transformer Overexcitation

A set of measurement signals monitored during the overexcitation is shown in the fig. 3.22.

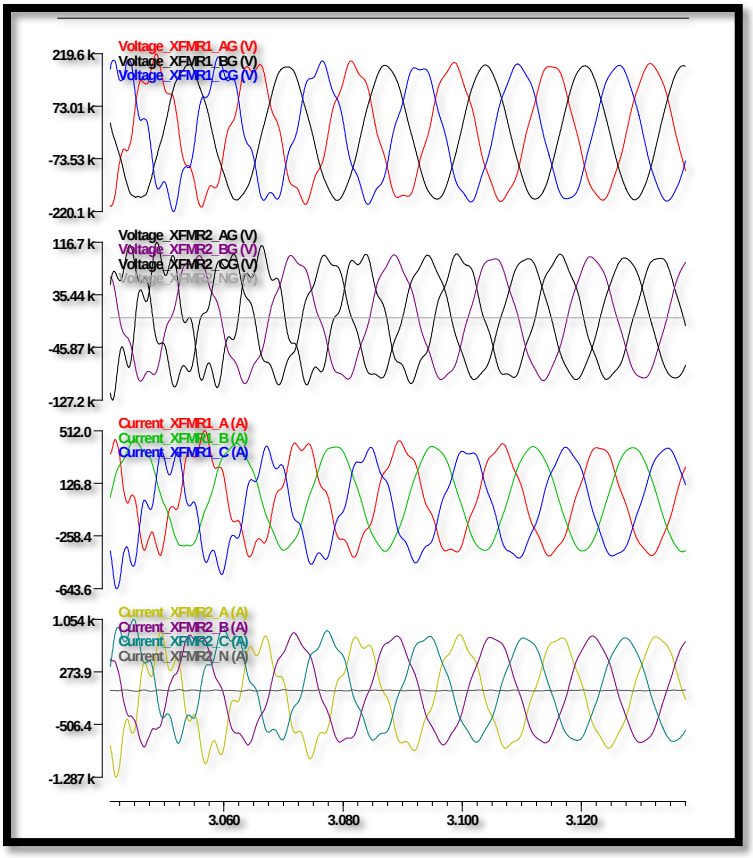

Figure 3.22: Measurement signals of the transformer (Test C: overexcitation)

Test D: Through Fault Condition

For through fault condition, the test system in fig. 3.18 is used, but single-phase-to-ground fault is given at a certain bus outside the transformer under protection. The fault lasts for 0.05 seconds, and then it is cleared. In fig. 3.23, the faulted location is marked with the red circle.

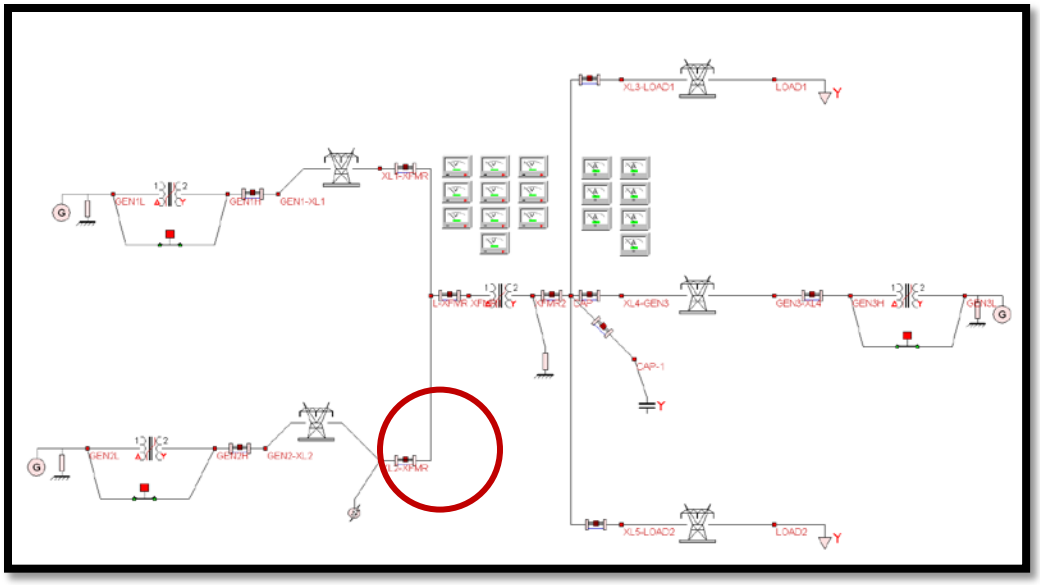

Figure 3.23: Fault location in the test system (test D: through fault)

A set of measurement signals monitored during the through fault condition is shown in the fig. 3.24. The single-phase-to-ground fault is given for 0.05 seconds, starting at 3.20 seconds.

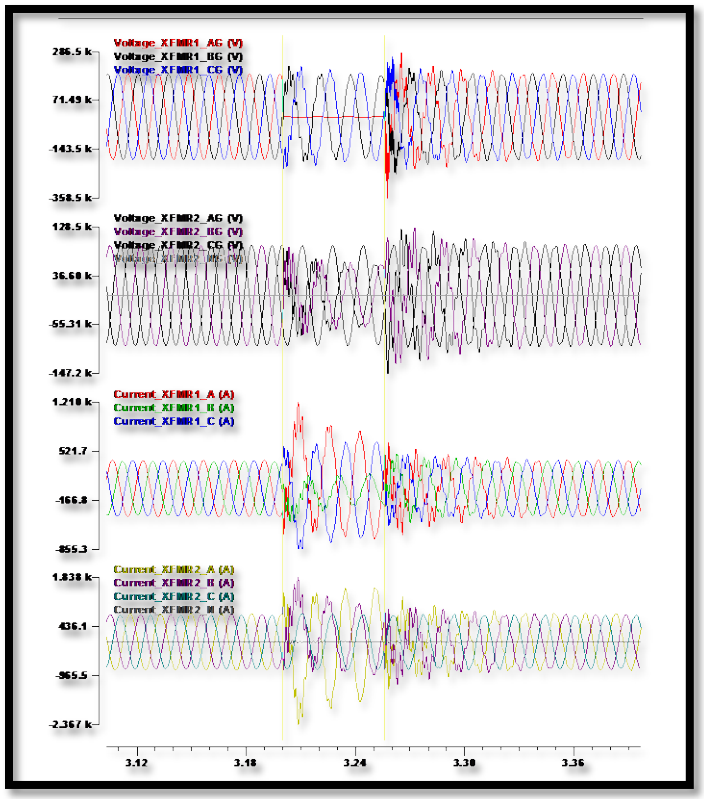

Figure 3.24: Measurement signals of the transformer (Test D: through fault)

Test E: Internal Fault Condition

For internal fault condition, the test system in fig. 3.18 is used.

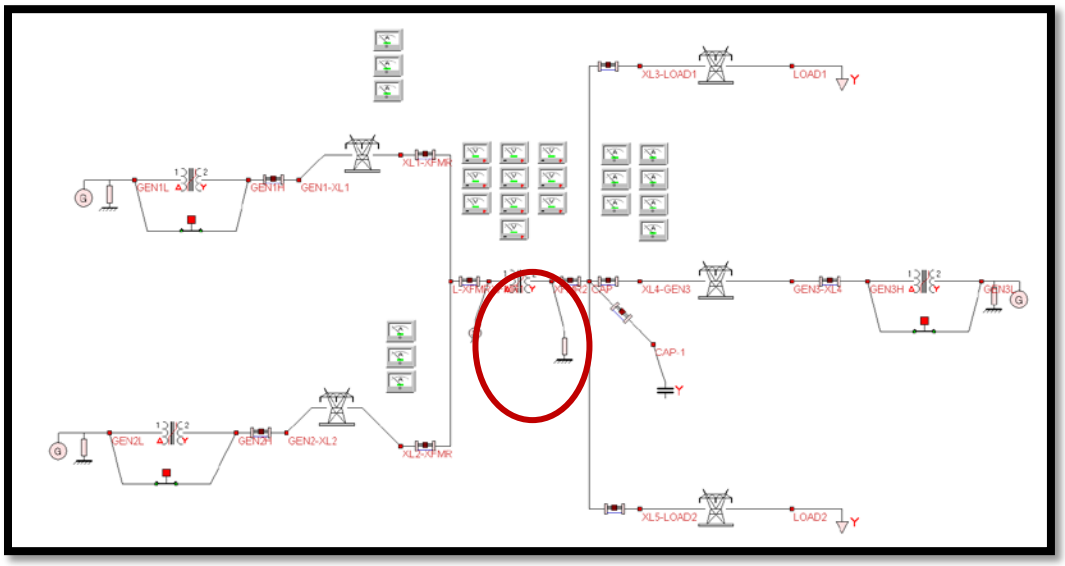

Figure 3.25: Fault location in the test system (Test E: internal fault)

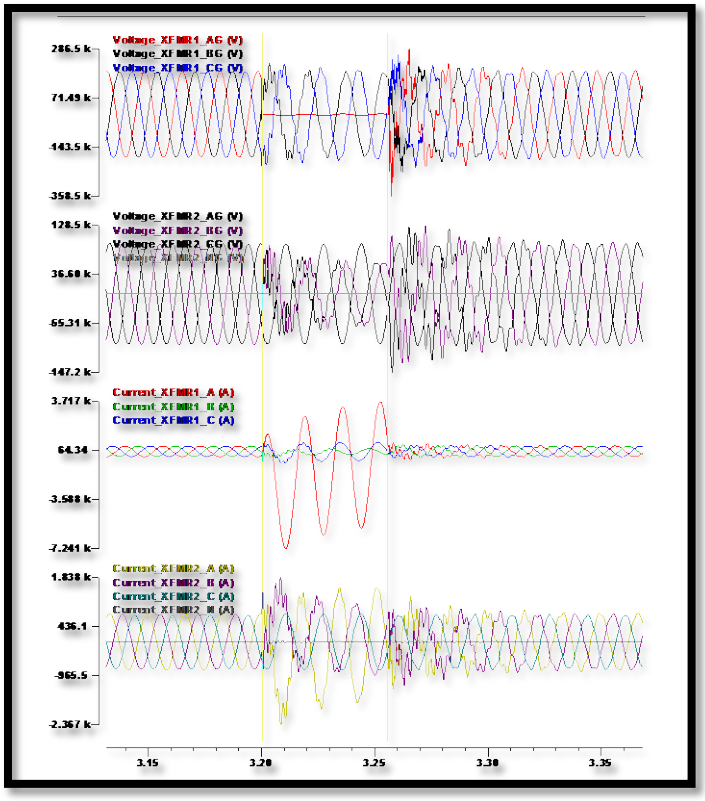

Figure 3.26: Measurement signals of the transformer (Test E: internal fault)

The single-phase-to-ground fault occurs at the phase-a terminal on the left side of the transformer for 0.05 seconds, and then the fault is cleared. In fig. 3.25, the faulted location is marked with the red circle.

A set of measurement signals monitored during the internal fault condition is shown in the fig. 3.26. To simulate the internal fault condition, the single-phase-to-ground fault is given inside the transformer (phase a) for 0.05 seconds, starting at 3.20 seconds.

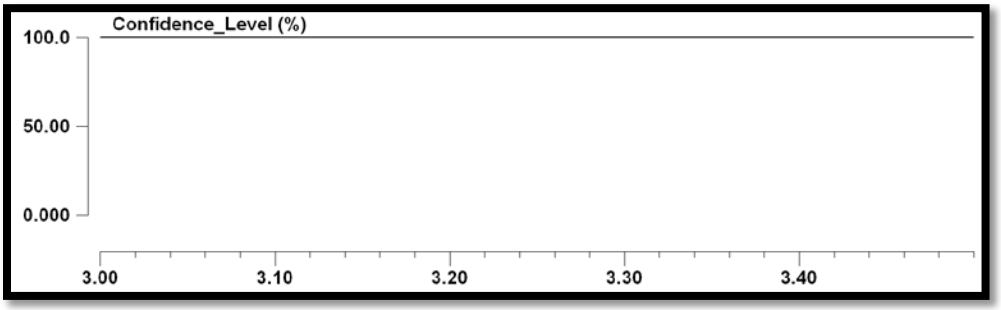

Figure 3.27: Confidence level of the DSE (Test A: normal operation)

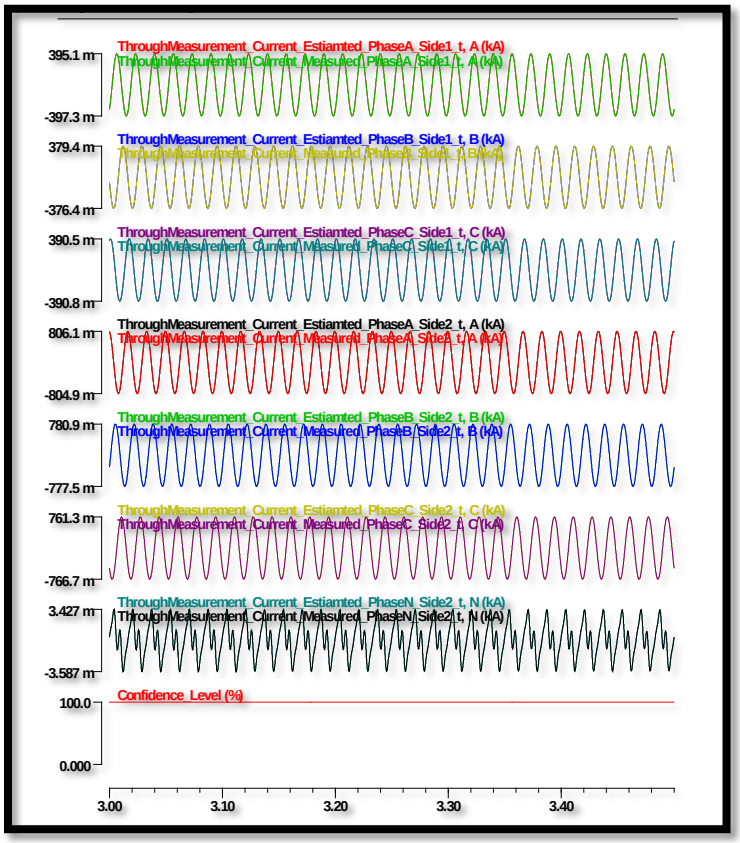

Figure 3.28: Current measurements, estimated values, and confidence level (Test A)

Performance Results for Test A: Normal Operating Condition

For the normal operating condition, the confidence level obtained by the developed dynamic state estimator has been shown in the fig. 3.27. The result graph shows 100% confidence level all the time, which means that measurements are consistent with the model and there is no fault condition during the simulation.
The measured and estimated currents at the primary and secondary side are compared with different colors as shown in the fig. 3.28.

The measured and estimated voltages are also compared in the fig. 3.29:

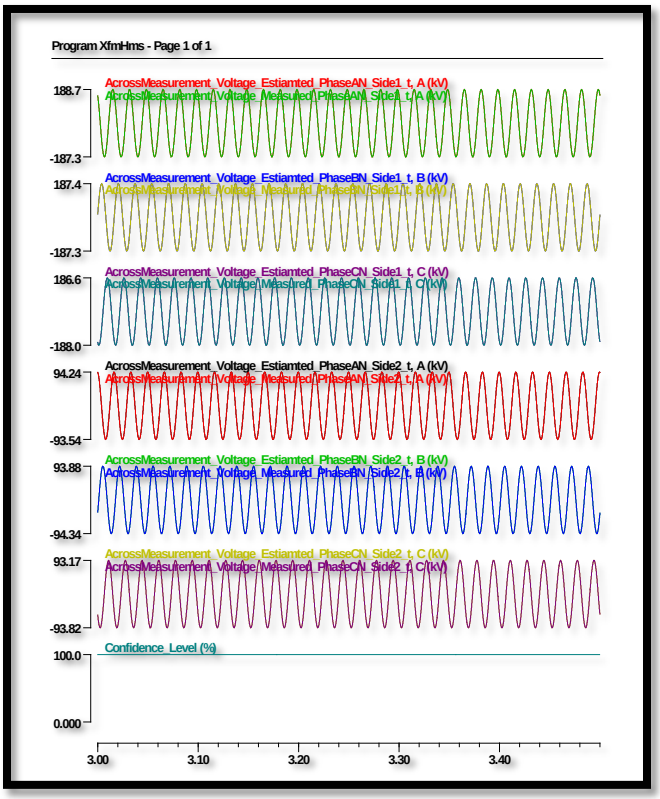

Figure 3.29: Voltage measurements, estimated values, and confidence level (Test A)

It can be concluded that the estimated voltages and currents are exactly same as the measured ones during the normal operation condition.

Performance Results for Test B: Transformer Energization (Inrush Current)

For the transformer energization, the confidence level obtained by the developed dynamic state estimator shows the fig. 3.30. The result graph shows 100% confidence level all the time, which means that measurements are consistent with the model and there is no fault condition during the simulation.

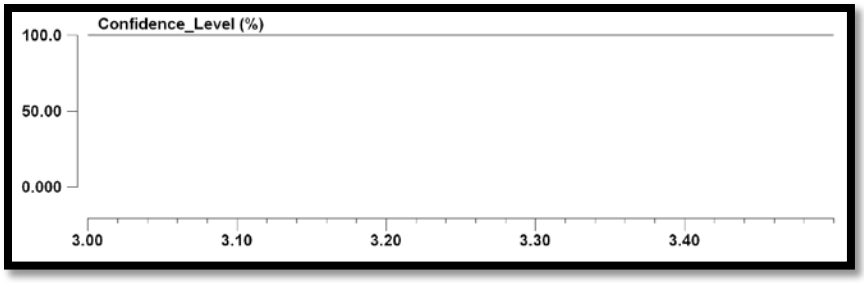

Figure 3.30: Confidence level of the DSE (Test B: transformer energization)

The measured and estimated currents at the primary and secondary side are compared with different colors as shown in the fig. 3.31.

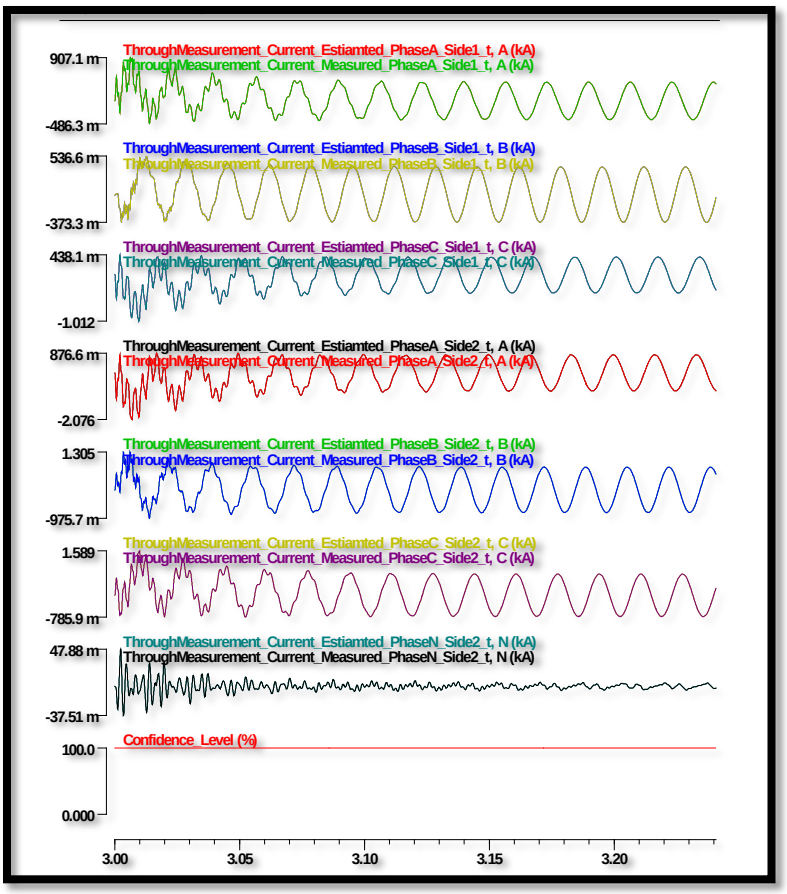

Figure 3.31: Current measurements, estimated values, and confidence level (Test B)

The measured and estimated voltages are also compared in the fig. 3.32.

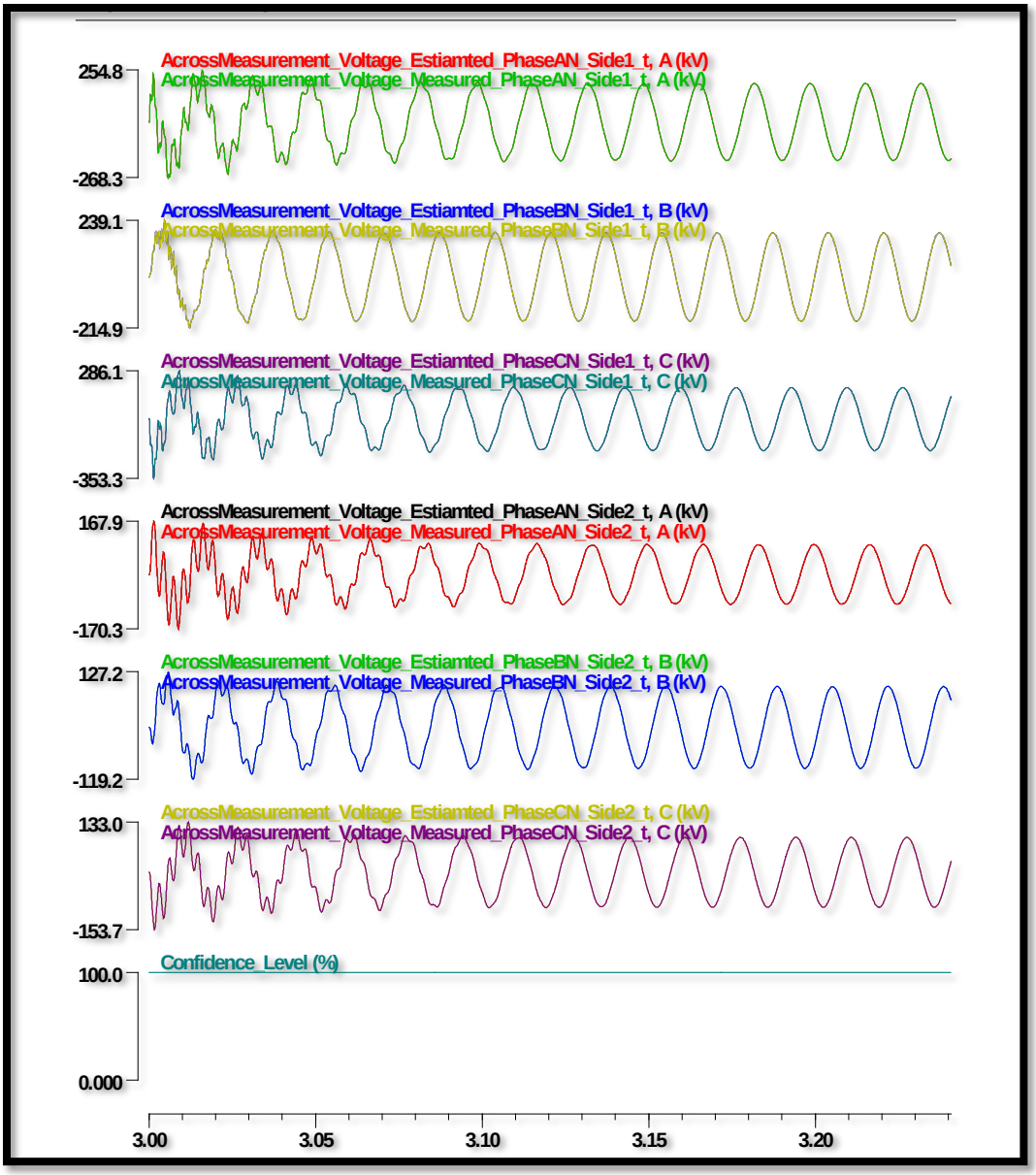

Figure 3.32: Voltage measurements, estimated values, and confidence level (Test B)

It can be concluded that the estimated voltages and currents are exactly same as measured ones during the normal operation condition.

Performance Results for Test C: Transformer Overexcitation

For the transformer overexcitation, the confidence level obtained by the developed dynamic state estimator is shown in the fig. 3.33. The result graph shows 100% confidence level all the time, which means that measurements are consistent with the model and there is no fault condition during the simulation.

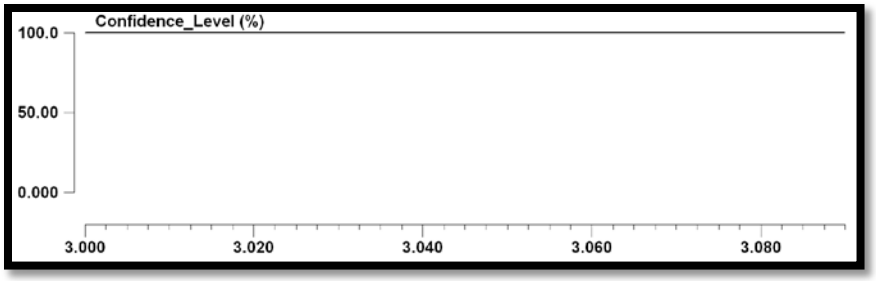

Figure 3.33: Confidence level of the DSE (Test C: transformer overexcitation)

The measured and estimated currents at the primary and secondary side are compared with different colors as shown in the fig. 3.34.

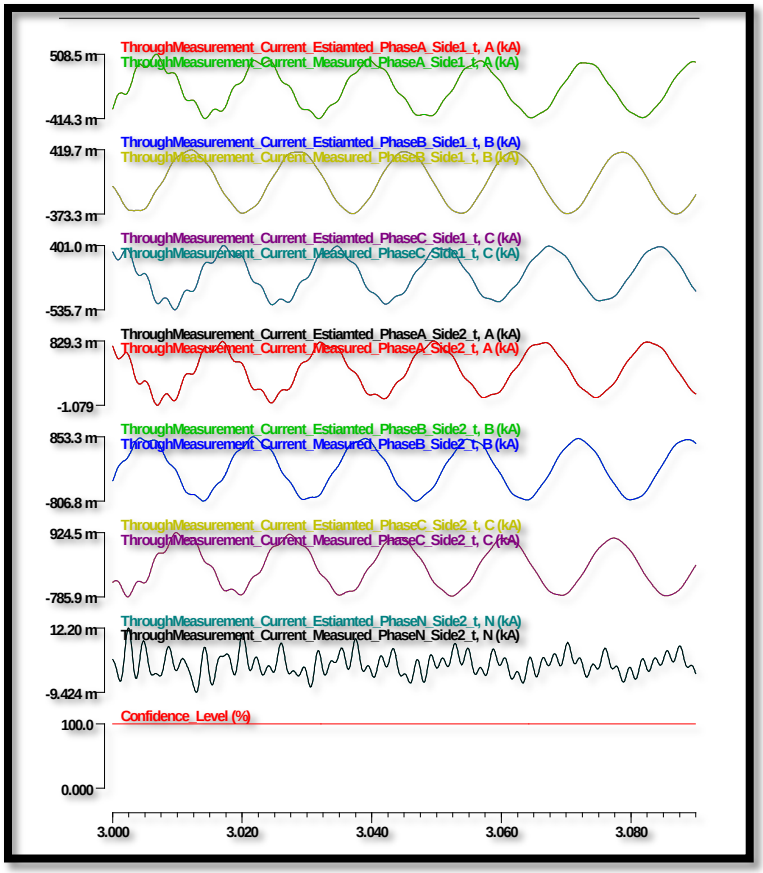

Figure 3.34: Current measurements, estimated values, and confidence level (Test C)

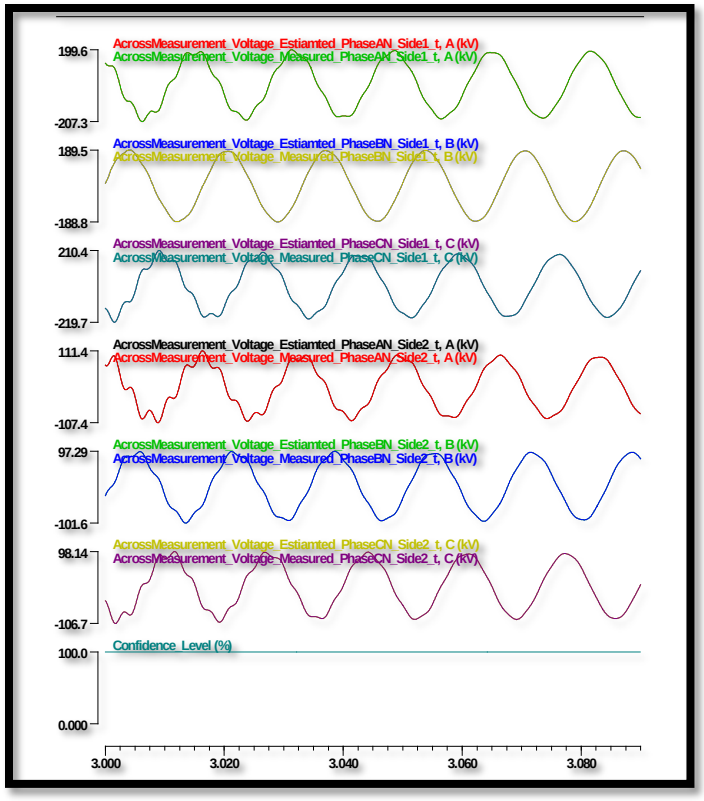

Figure 3.35: Voltage measurements, estimated values, and confidence level (Test C)

The measured and estimated voltages are also compared in the fig. 3.35.

It can be concluded that the estimated voltages and currents are exactly same as measured ones during the normal operation condition.

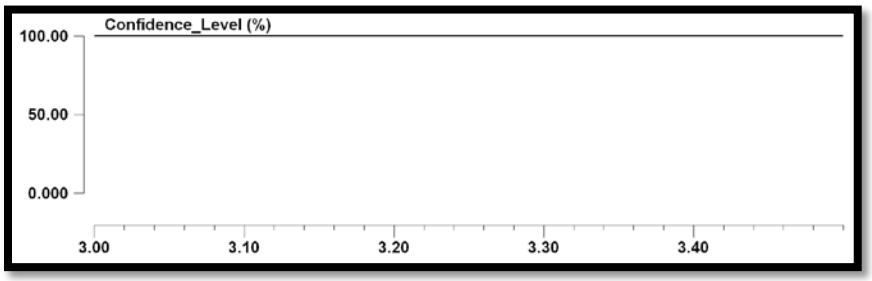

Figure 3.36: Confidence level of the DSE (Test D: through fault)

Performance Results for Test D: Through Fault Condition

For the through fault condition, the confidence level obtained by the developed dynamic state estimator is shown in the fig. 3.36. The result graph shows 100% confidence level all the time, which means that measurements are consistent with the model and there is

no fault condition during the simulation. The measured and estimated currents at the primary and secondary side are compared with different colors as shown in the fig. 3.37.

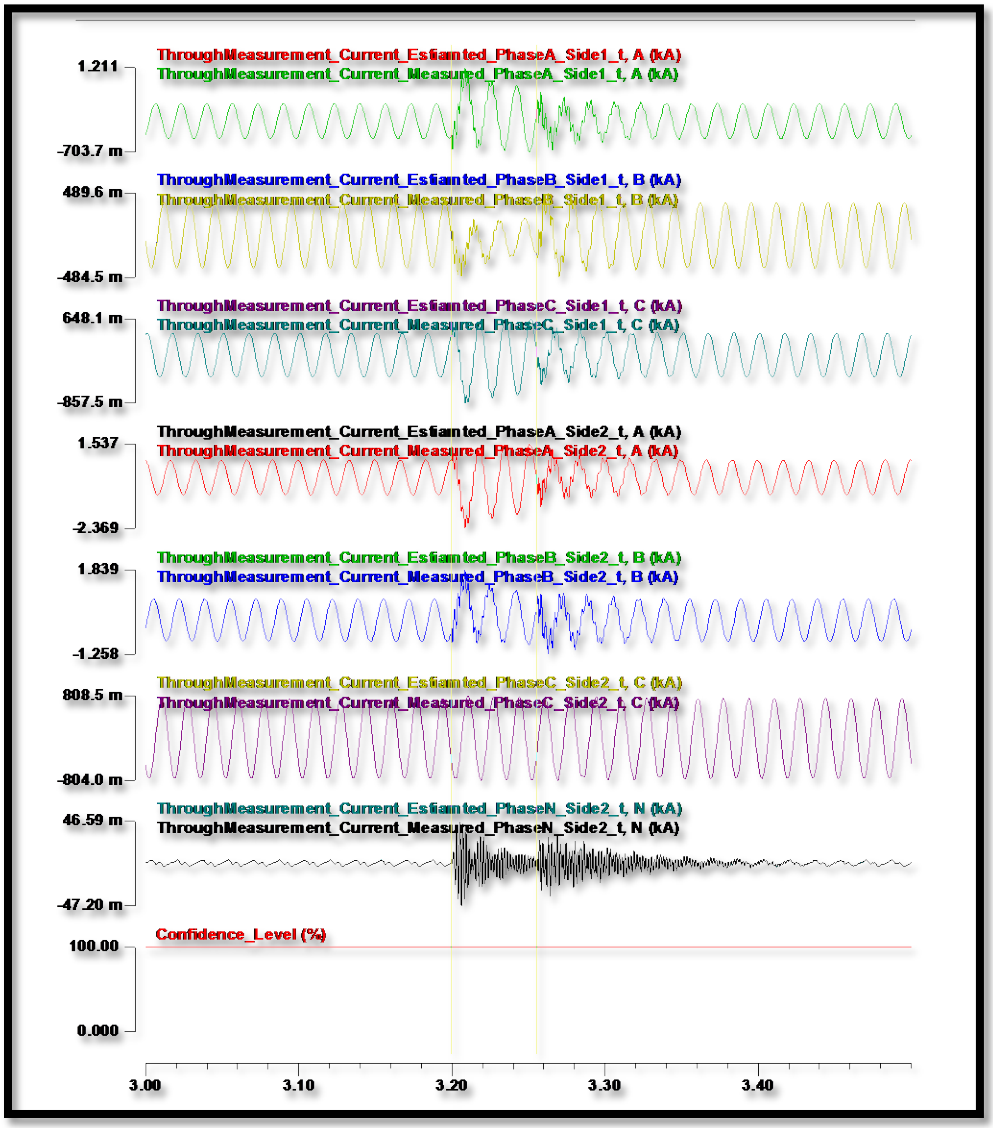

Figure 3.37: Current measurements, estimated values, and confidence level (Test D)

The measured and estimated voltages are also compared in the fig. 3.38.

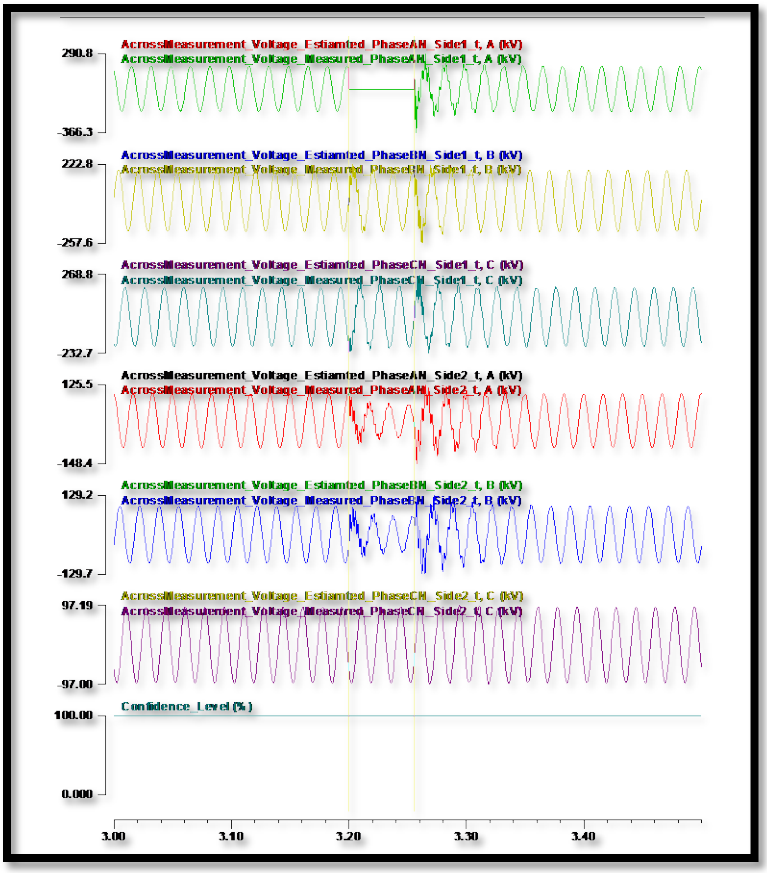

Figure 3.38: Voltage measurements, estimated values, and confidence level (Test D)

Performance Results for Test E: Internal Fault Condition

For the internal fault condition, the confidence level obtained by the developed dynamic state estimator is shown in fig. 3.39. During most of the time, the confidence level is 100%, which means that measurements are consistent with the model. However, at time 0.2 second in fig. 3.39, the confidence level drops to 0%, which means that an internal fault has occurred somewhere in the transformer. Then, the confidence level recovers 100% in 0.05s as the transformer returns to the normal operating condition.

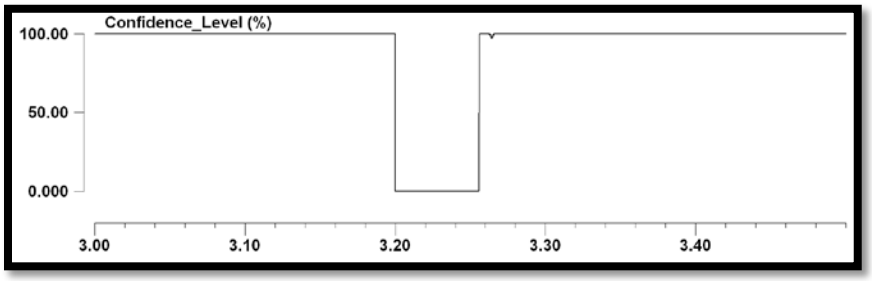

Figure 3.39: Confidence level of the DSE (Test E: internal fault)

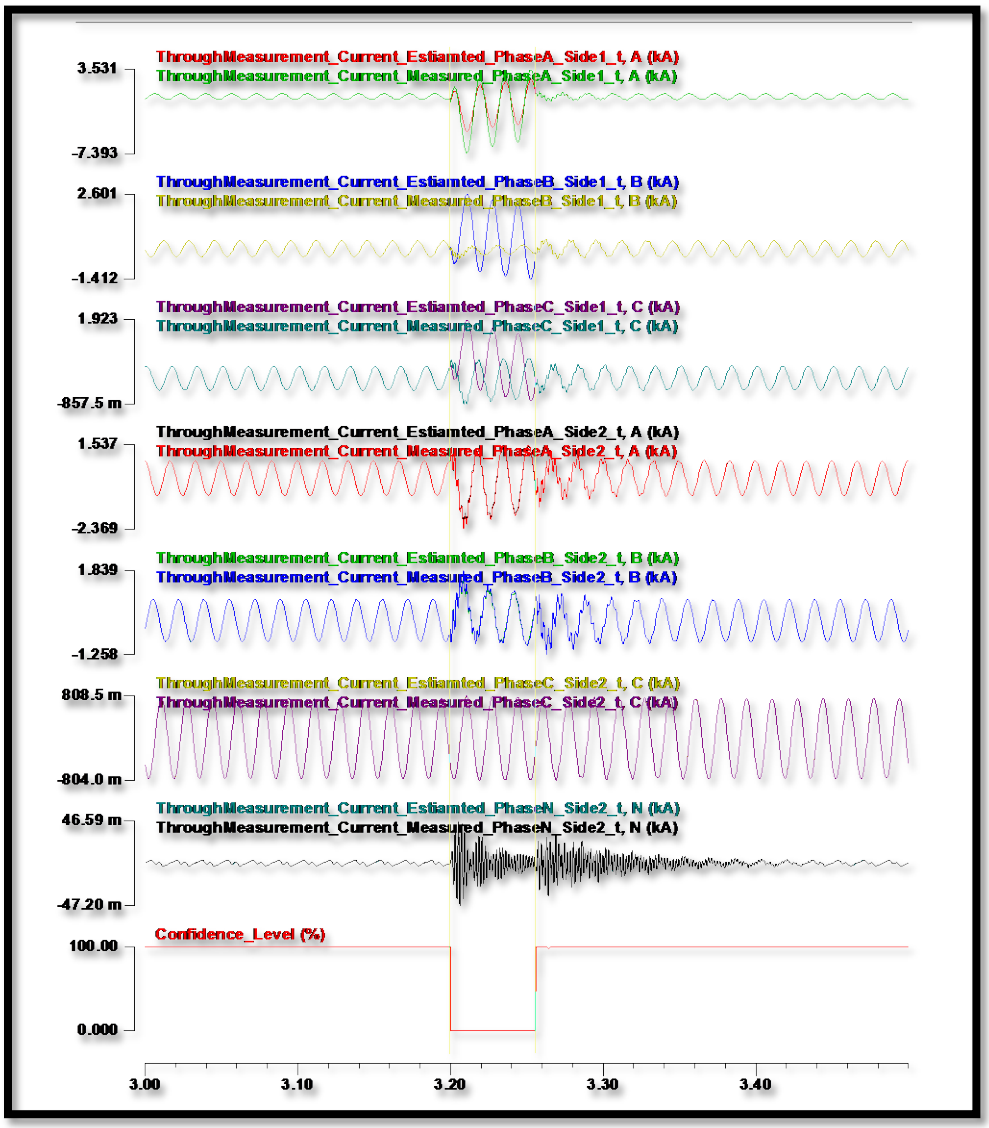

Figure 3.40: Current measurements, estimated values, and confidence level (Test E)

The measured and estimated currents at the primary and secondary side are compared with different colors as shown in the following fig. 3.40.
The measured and estimated voltages are also compared in the following fig. 3.41.

Note that there is a specific duration in which the confidence level is zero, and therefore, it can be concluded that any internal faults have occurred in the transformer under protection during this period.

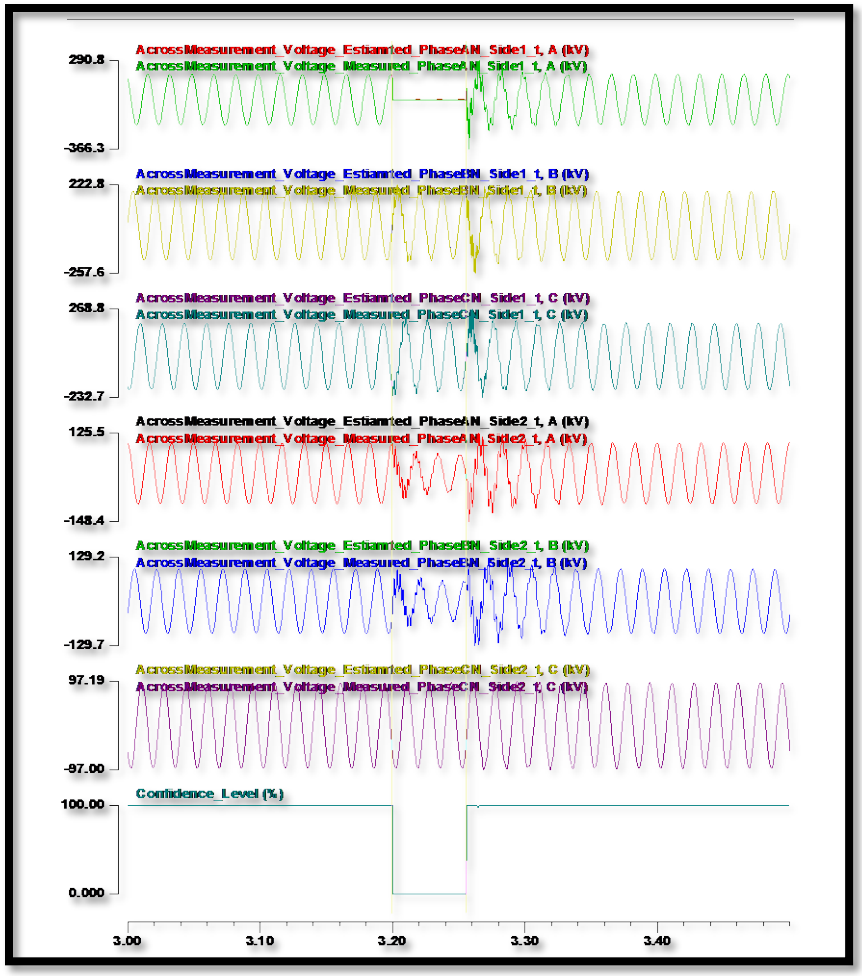

Figure 3.41: Voltage measurements, estimated values, and confidence level (Test E)

3.3.5 Conclusions on DSE Based Transformer Protection

The setting-less protection approach based on dynamic state estimation for the 3-phase transformer has been proven to be a reliable method to protect the transformer against internal faults. It was shown that the relay does not trip during normal operating conditions or faults outside the protection zone. On the other hand, a trip is decided during the internal fault. The simulation results verify the theoretical analysis. The computation time needed is within the requirements of the data acquisition scheme.

4 Conclusions and Future Research Direction

4.1 Conclusions

Synchrophasor technology enables real time monitoring and control of power grid. However, before putting the smart devices and algorithms in use in the actual power grid, it is important to test and validate their capabilities as well as their accuracy. The motive is to ensure high accuracy of measurements from synchrophasor devices and the validation of developed algorithms utilizing synchrophasors, under different operating scenarios of the power system. This research project report provide details for testing of synchrophasor devices, testing of phasor based voltage stability and state estimation applications as well as utilization of PMUs for advanced protection schemes with emphasis on dynamic protection algorithms for transformers.

To perform testing of synchrophasor devices and applications, Real Time Digital Simulator (RTDS) based testing facility at Washington State University (WSU) and WinIGS-T based testing facility at Georgia Institute of Technology (GIT) have been utilized. Test systems and library of test conditions have been developed based on IEEE C37.118.1 standard. Standard PMU was modeled as a benchmark phasor measurement unit (PMU).

PMU steady state performance test results for range of magnitude changes show that for nominal frequency and balanced system, total vector error for voltage and current are within the limit. The current TVEs of all the 3 phases are not the same and more than voltage TVE. Frequency Error (FE) and rate of change of frequency error is much below the allowed threshold value. For off nominal frequency, voltage TVE and current TVE are higher than 1%. FE and RFE mostly stay within specified limit. With harmonics, voltage and current TVE are within limit. RFE and FE is higher, when harmonics are present, but within the specified limit. With off-nominal and harmonics, voltage TVE and current TVE are higher than 1% limit. FE and RFE still remain within limit. For steady state, range of angle changes test conditions reveal that for nominal frequency and balanced system, voltage and current TVE as well as FE/ RFE are within the limit. With harmonics introduced, current TVE are higher than allowed limit while voltage TVE, Fe and RFE are within the limit. For off-nominal frequency, current TVE and voltage TVE are more than 1%, while FE and RFE stays within specified limit.

For dynamic testing, most of the tested PMUs failed the performance criterion. For magnitude and angle step change, tested PMU meets the requirement of response time and overshoot but not the delay time. For frequency step change, PMU meets the requirement of frequency response time and overshoot but does not meet the requirement of ROCOF response time and delay time. PMU does not meet the requirement of FE and RFE for the frequency ramp change. For amplitude phase and frequency modulation test, performance criterion were not met for voltage TVE, current TVE, FE and RFE. From the analysis of the steady state and dynamic tests, it can be seen that the PMU under test behaves differently under different system conditions. The tests performed on the PMU

under test provides a comprehensive coverage of the performance criterion for the PMU. PMU under test satisfies most of the test criteria as mentioned in the standard for steady state, but fails some of them in dynamic testing.

For testing of phasor data concentrator, test scenarios were developed for data alignment, data validation, data loss, data latency, data rate conversion, format conversion as well as phase/ magnitude compensation. All the PDC tested passed data alignment and data validation test for the different durations and reporting rate of data streaming, collection and archival. PDC also passed the data loss test unless data is being transferred through complex communication network. Tested PDC gave satisfactory performance for data latency, data rate conversion, format conversion and phase/ magnitude compensation.

For synchrophasor applications testing, functionalities for specific voltage stability algorithm, state estimators and dynamic protection algorithms for transformers were tested. Goal was to validate real time performance of these algorithms in lab environment before installing in industry. Test bed with real time digital simulator, hardware PMUs, modeled PMUs, PDC, real time controllers, network simulator-3 and number of computers were integrated to create real system environment. Voltage stability algorithm was simulated using real time digital simulators, number of PMU's and controllers. Expected performance and feasibility for real time application were verified for line outage and loading condition change. For dynamic state estimation, it performed very well with transformer inrush current, overexcitation, and fault conditions. The setting-less protection approach based on dynamic state estimation for the 3-phase transformer has been proven to be a reliable method to protect the transformer against internal faults. It was shown that the relay does not trip during normal operating conditions or faults outside the protection zone. On the other hand, a trip is decided during the internal fault. The computation time needed is within the requirements of the data acquisition scheme and suitable for real time applications.

This project contributed towards developing better dynamic protection algorithm for transformer, test suites and framework for performance testing of PMUs/ PDCs, as well as test bed for evaluation of PMU based applications including voltage stability and state estimation in real time. This project helped one of the graduate students to get internship at Southern California Edition to work on tool development for automating testing and report writing for PMU testing based on IEEE C37.118.1 standard. Other participants in this project played a key role as member of IEEE standard development and forming IEEE PMU conformance committee for certification. This project also helped the project leader to organize first synchrophasor testing and validation workshop at Washington State University.

4.2 Future Research Directions

Developed test bed provides necessary framework to test number of other possible synchrophasor applications such as oscillation monitoring, remedial action scheme, parameter estimation, event analysis and real time control. Tested application in real time

will provide ready to deploy algorithms for pilot phase. Test bed also provides excellent platform for synchrophasor education.

Performance results reported here for PMU and PDC can be used as a guideline for the modification and development of the standards. Results also provide insight to vendors for available PMUs and guidance for designing future PMUs. Test results also shows need for additional algorithms to filter out bad data for applications related to transients and dynamics as well as real time control. Dynamic protection algorithms for transformer protection can be incorporated in new relays with PMU capability.

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