



Efficient Modeling of Modular Multilevel Converters for Fast Simulation of Large-Scale MMC-HVDC Embedded Power Systems

Final Project Report

S-78G

Power Systems Engineering Research Center
*Empowering Minds to Engineer
the Future Electric Energy System*



Efficient Modeling of Modular Multilevel Converters for Fast Simulation of Large-Scale MMC-HVDC Embedded Power Systems

Final Project Report

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PSERC Publication 18-05

September 2018

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Acknowledgements

This is the final report for the Power Systems Engineering Research Center (PSERC) research project titled “Efficient Modeling of Modular Multilevel Converters for Fast Simulation of Large-Scale MMC-HVDC Embedded Power Systems” (project S-78G). We express our appreciation for the support provided by PSERC’s industry members. In particular, this work was support by GEIRINA and we wish to thank the industry advisors for this project: Zhiwei Wang, Di Shi, and Xi Chen.

Executive Summary

Modular multilevel converter (MMC) has become the most attractive multilevel converter topology for voltage-sourced converter high-voltage direct current (VSC-HVDC) transmission systems. The salient features of MMC include: 1) modularity and scalability to meet any voltage level by stacking up additional numbers of SMs without increasing topology complexity, 2) inherent redundancy and fault-tolerance capability to improve reliability, 3) high efficiency suitable for high-power applications, and 4) high power quality and low filter/transformer cost due to filter-free and transformerless applications by realization of high-level converters. With the increasing number of the MMC-HVDC systems embedded into ac grids, the performance of the present power systems may be dramatically improved, including stability, reliability, capacity, and efficiency. However, the MMCs' applications are restricted due to several important technical challenges. One of the major challenges is to effectively and accurately model various MMCs for fast simulation of large-scale power systems. In this report, an equivalent circuit model (ECM) is proposed for modeling and simulating the MMCs based on various submodule (SM) circuits and arm configurations. The proposed ECM can significantly improve simulation efficiency and be applied for precharging, normal, and fault operation analysis of the MMC-HVDC systems while considering the behaviors of various SM circuits. The proposed accelerated model can also be used to investigate internal dynamics with various control strategies, e.g., capacitor voltage balancing, when full states are considered. To further improve efficiency, the proposed model can be implemented by the reduced-order algorithm. The effectiveness of the proposed ECM is verified by an MMC-HVDC system built in PSCAD/EMTDC software environment. Also, the proposed ECM is applicable for other simulation platforms.

Problems of the Existing Models

The MMC with half-bridge (HB) SMs is the dominant topology for HVDC systems due to its low cost and low loss. However, in case of a dc-side short-circuit fault, the HB-MMC cannot block the fault currents fed from ac grid. Therefore, various SMs have been proposed and investigated to improve the fault blocking capability of the MMCs, such as the full-bridge (FB), unipolar-voltage full-bridge (UFB), clamp-double (CD), and three-level/five-level cross-connected (3LCC/5LCC) SMs. These fault-blocking SMs can block the fault current fed from ac grids. For large-scale MMCs-embedded power systems, it is required to investigate dynamic performance, fault, protection, and stability. The conventional detailed switching model (DSM) is time consuming and infeasible due to the large number of semiconductor switches in high-level systems. To address this challenge, several MMC models have been developed to accelerate the electromagnetic transient (EMT) simulation. However, the existing models are usually developed for some specific SM circuits and certain operating conditions. They also do not consider bipolar arm voltages and static compensator (STATCOM) operating conditions during a fault.

The Proposed Equivalent Circuit for Modeling the MMCs

To consider various SM circuits and different operating conditions, a generalized equivalent circuit of an arm of the MMC is proposed. The proposed equivalent arm circuit consists of a controllable voltage source, four controllable switches, and four diodes. By properly switching

on and off the four switches, the proposed circuit can simulate the behaviors of various SM circuits, i.e., the HB, FB, UFB, CD, 3LCC, and 5LCC SMs under different operating conditions, including startup, normal, and fault operations. Therefore, based on the proposed equivalent arm circuit, the MMCs with various configurations can be modeled in a general way and simulated for efficiently analyzing large-scale hybrid ac and dc power systems.

In this study, several operating conditions will be considered, including precharging/startup condition, normal, and fault conditions. Under the precharging/startup condition, the SM capacitors will be charged to the nominal voltage. For normal operation, the internal dynamics of the MMCs should be controlled properly. During a dc fault, all semiconductor switches of the MMCs are turned off; the HB SM cannot block the fault current while the fault-blocking SMs can produce negative voltages against the ac-side voltages so that the fault current can be blocked.

To accurately investigate the internal dynamics of the MMCs, all capacitor voltages should be considered to evaluate the applied control strategies. This detailed ECM is solved by calculating all SM capacitor voltages to estimate each arm voltage. The detailed ECM needs capacitor voltage balancing strategy and is applicable for evaluating the performance of the practical control algorithms, e.g., power flow control, capacitor voltage balancing, circulating current control, and startup control. To further improve the computational efficiency of modeling and simulating large-scale MMC-based hybrid ac and dc systems, the proposed ECM can be modified by reducing the number of state variables, i.e., capacitor voltages. This reduced-order ECM assumes that all capacitor voltages are well balanced and only the average capacitor voltage of each arm is considered to calculate the arm voltage.

Performance Evaluation and Verifications

To verify the proposed ECM, a point-to-point MMC-HVDC system is selected as the study system and built in PSCAD/EMTDC program environment. Various MMC configurations based on different SM circuits are modeled and simulated under different operating conditions to evaluate the performance of the proposed modeling technique. The simulation results show that the proposed ECM can accurately and efficiently model and simulate the MMC-based systems for various SM circuits and arm configurations under different operating conditions. For the study cases, the simulation run time can be reduced from several or tens of thousands seconds to tens of seconds. With the conventional DSM, the SMs with more complex circuit topology have longer runtime. However, by using the proposed ECM, the run time is not related to the circuit topology complexity. The run time is determined by the number of voltage levels. For the proposed reduced-order ECM, there is no significant increase in run time when the voltage level is low. In addition, the STATCOM mode under dc fault condition can be implemented based on the proposed ECM.

Conclusions

- The proposed ECM can significantly improve simulation efficiency (speed) while keeping enough accuracy.
- The complexity of SM circuit topology significantly influences the simulation run time for the conventional detailed switching model. However, there is no significant impact of SM circuit topology on the run time of the proposed ECM.
- The run time of the proposed ECM increases with the increasing number of voltage levels.

Project Publications:

- [1] L. Zhang, J. Qin, D. Shi, and Z. Wang, "Efficient modeling of hybrid MMCs for HVDC systems," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 1629-1633.
- [2] L. Zhang, J. Qin, D. Shi, and Z. Wang, "An Improved Equivalent Circuit Model of MMC and Influence Analysis of Simulation Time Step," *IEEE Transactions on Power Delivery*, in preparation.

Student Theses:

- [1] Lei Zhang. *Modeling and Control of Modular Multilevel Converters for High-Power Applications*. PhD dissertation, Arizona State University, Tempe AZ, expected in January 2020.

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1. Introduction

1.1 Background

Due to modularity and scalability, modular multilevel converter (MMC) has become the most attractive converter topology for medium/high voltage applications, especially for voltage-sourced converter high-voltage direct current (VSC HVDC) transmission systems [1]. The MMC with half-bridge (HB) submodules (SMs) is the dominant topology for HVDC systems due to its low cost and low loss. However, in case of a dc-side short-circuit fault, the HB-MMC cannot block the fault currents fed from ac grid. Various SMs have been proposed and investigated to improve the fault blocking capability of the MMC, such as the full-bridge (FB), unipolar-voltage full-bridge (UFB), clamp-double (CD), and three-level/five-level cross-connected (3LCC/5LCC) SMs [2]–[4].

1.2 Overview of the Problem

For large-scale MMCs-embedded power systems, it is required to investigate dynamic performance, fault, protection, and stability [5]–[8] through modeling and simulation. However, the conventional detailed switching model (DSM) is time consuming and infeasible due to the large number of semiconductor switches in high-level systems. To address this challenge, several MMC models have been developed to accelerate the electromagnetic transient (EMT) simulation.

- Averaged models: In [9], [10], an average model has been proposed for the HB-MMC under normal operating conditions, without considering dc fault conditions. Reference [11], presents two average-value models for the HB-MMC-MTDC systems. As discussed in [11], although they are scalable and efficient, they are not applicable for dc-side transient and fault conditions. Similar models are also presented for the HB-MMC and the FB-MMC in [8], [12], [13].
- Detailed equivalent circuit models (ECMs): To investigate dc fault conditions, a detailed ECM combined with a hybrid HVDC breaker is proposed in [14] for the HB-MMC-MTDC system, which is able to estimate the dynamics of each capacitor voltage. The switching function of each SM and arm currents are required to calculate the capacitor voltages and arm voltages based on numerical methods.
- ECMs with fault-blocking capability: The aforementioned models are proposed for the HB-MMCs, which do not have fault blocking capability. To consider the MMC with embedded fault-blocking capability, a detailed ECM has been proposed for self-blocking MMC (SB-MMC) in [15]. However, the proposed ECM is only specified for the SB-MMC. Reference [16] presents an ECM for hardware-in-the-loop (HIL) test bench, which is suitable for the HB-MMC and FB-MMC.

To consider various SM circuits and different arm configurations under different operating conditions, in this project, a generalized ECM is proposed to model and simulate the MMC-based HVDC systems and dc grids for analyzing large-scale hybrid ac and dc systems.

1.3 Report Organization

This report is structured as follows. Chapter 2, briefly introduces the operational principles of the MMCs based on various SMs. Then a generalized ECM is proposed and analyzed in Chapter 3. In Chapter 4, the proposed ECM is verified by the simulation model built in PSCAD/EMTDC program environment. Chapter 5 concludes this project.

2. Operational Principles of the MMCs with Various SMs

2.1 Operational Principles of the MMCs

A schematic diagram of the MMC and various SM circuits are shown in Fig. 2.1. In this project, several operating conditions will be considered, including precharging/startup, normal, and fault conditions.

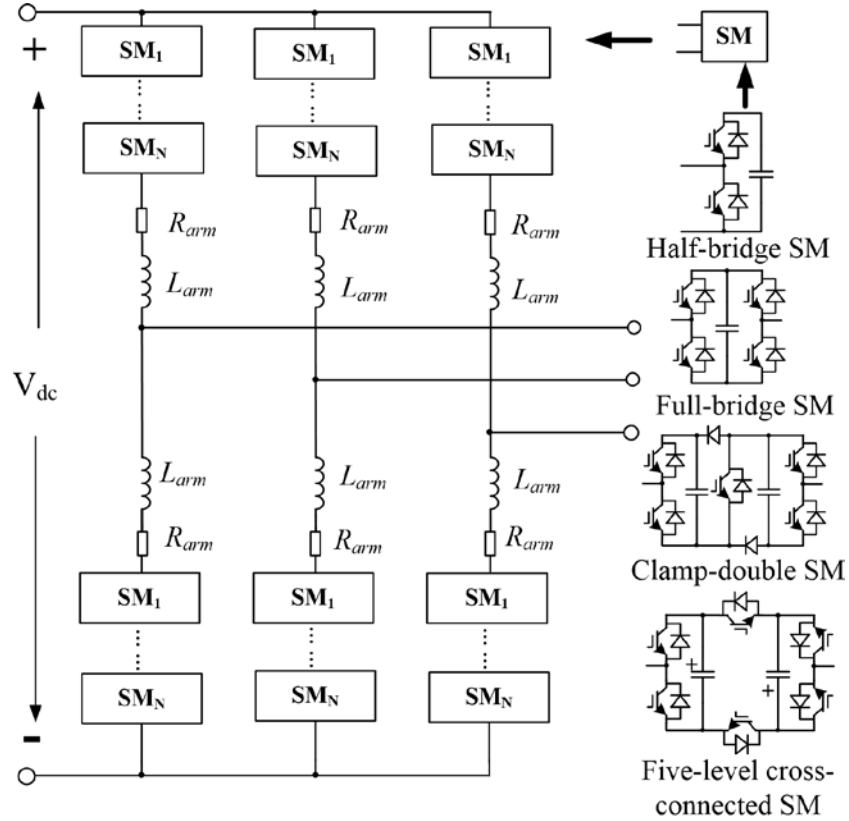


Figure 2.1 Block diagram of the MMC and various SM circuits.

- Precharging/startup condition: Before normal operating condition, the SM capacitors should be charged to the nominal voltage. The precharging strategies have been investigated in [17]–[19]. Reference [19] proposes a generalized startup process for various MMC-HVDC systems, which will be used as the startup method in this project. In the uncontrollable precharging stage, the current from either ac or dc side flows through the anti-parallel diodes of semiconductor switches and charges the SM capacitors to a steady-state voltage. When the SMs become controllable, the number of the inserted capacitors are properly controlled to charge the capacitor voltages to their nominal value.
- Normal operating condition: The basic operational principles of the MMCs have been presented in [1], [20], [21], in which the SM configurations, modulation methods, mathematical model, and design constraints have been investigated. Each arm can be simplified as a controllable voltage source. The ac-side currents and circulating currents can be controlled by controlling the arm voltages.

- DC fault condition: When the dc fault occurs, all controllable switches are turned off. The HB SM cannot block the fault current due to the current flowing through the anti-parallel diodes. On the other hand, the fault-blocking SMs produce negative voltages against the ac-side voltages so that the fault current can be blocked. The fault current paths of various SMs are shown in Fig. 2.2. Therefore, the MMCs based on various SM circuits have different dynamic behaviors, which should be considered in modeling and simulation of the MMC-based systems.

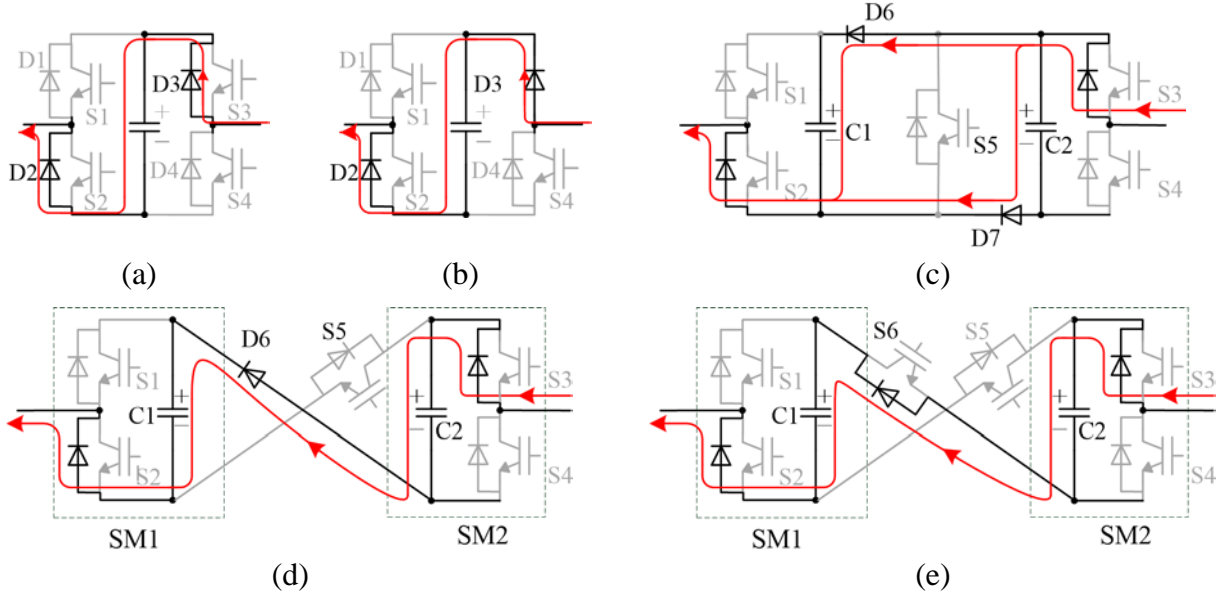


Figure 2.2 The fault current paths of various SMs: (a) FB, (b) UFB, (c) CD, (d) 3LCC, and (e) 5LCC SM circuits.

2.2 SM Operations

For the HB SM, there are three operating states: inserted, bypassed, and blocked [18], [22]. For the fault-blocking SMs [2]–[4], when the proper switches (i.e., conducting switches) are turned on/off, they operate like the HB SM:

- UFB and FB: When S4 in the UFB SM and S3 or S4 in the FB SM are turned on, the UFB SM and FB SM can operate as the same behavior of the HB SM.
- CD, 3LCC, and 5LCC: When S5 in the CD and 3LCC SMs and S5 or S6 in the 5LCC SM are turned on, these SMs operate like two independent HB SMs.

3. The Proposed ECM for Various SMs and Arm Configurations

To consider the aforementioned various operating conditions and SM circuits, a generalized equivalent circuit model (ECM) of an arm of the MMC is proposed and shown in Fig. 3.1. It consists of a controllable voltage source, two controllable switches, and four diodes. The proposed equivalent circuit of an arm can be used to model and simulate the MMCs based on the HB SMs, the fault-blocking SMs, or the combination of various SMs under different operating conditions.

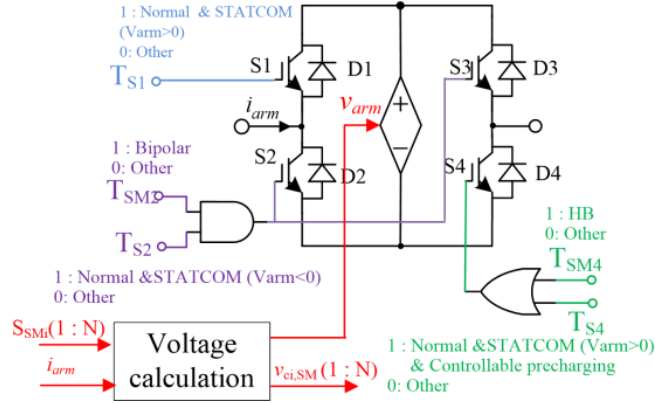


Figure 3.1 The proposed equivalent circuit of an arm.

3.1 Switching States of the Equivalent Arm Circuit

The switching states of the proposed equivalent arm circuit depend on MMC configurations and operating conditions.

3.1.1 Modeling of the HB-MMC

To model and simulate the HB-MMC, S4 in the equivalent arm circuit of Fig. 3.1 is always on. For various operating conditions, the proposed ECM in Fig. 3.1 operates as follows:

- Precharging/startup and dc-fault conditions: S1 is turned off and S4 is always on. The current paths are shown in Fig. 3.2.
- Normal operating condition: Under normal operating condition, both S1 and S4 are turned on. Either the positive or negative arm current flows through the controllable voltage source of Fig. 3.2.



Figure 3.2 Current paths of the proposed ECM for the HB-MMC under precharging and dc fault conditions: (a) positive arm current, and (b) negative arm current.

3.1.2 Modeling of the MMCs containing the fault-blocking SMs

To model and simulate the MMCs that consist of the fault-blocking SMs, the proposed ECM of Fig. 3.1 operates as follows:

- Uncontrollable precharging and fault conditions: If the fault-blocking SMs are all blocked, the arm current flows through the anti-parallel diodes of the switches to charge the SM capacitors. The current paths are shown in Fig. 3.3.
- Controllable precharging condition: When the conducting switches are turned on, the fault-blocking SMs have the same behaviors of the HB SM. Under this condition, S4 is on and S1 is off.
- Normal operating condition: Both S1 and S4 are turned on.



Figure 3.3 Current paths of the proposed ECM for the FB-MMC under precharging and dc fault conditions: (a) positive arm current, and (b) negative arm current.

For the hybrid MMCs based on the HB and the fault-blocking SMs, the switching states of the proposed ECM are the same as that of the MMCs based on the fault-blocking SMs. The difference is the calculation of the controllable voltage source, which will be discussed in following chapters. For various MMC configurations and operating conditions, the switching states of the proposed ECM of Fig. 3.1 are listed in Table 3.1.

Table 3.1
Operating modes and switching states of the proposed ECM

Operating condition		SM	S1	S2	S3	S4
Precharging	Uncontrollable	HB	0	0	0	1
		Others	0	0	0	0
	Controllable	All	0	0	0	1
Normal & Fault-STATCOM		HB	1	0	0	1
		Others	1	0	0	1
DC fault		HB	0	0	0	1
		Others	0	0	0	0

3.2 The Proposed Detailed ECM

Based on the proposed ECM, the detailed model is solved by calculating all SM capacitor voltages to estimate the arm voltage V_{arm} of Fig. 3.1. The detailed ECM needs capacitor voltage balancing strategies and is suitable for investigating the internal dynamics of the MMCs. To determine V_{arm} , the capacitor voltages in each arm are estimated and V_{arm} is the sum of the estimated capacitor voltages.

3.2.1 Capacitor voltage

The dynamics of each capacitor voltage is described by

$$i_c = C \frac{dv_c}{dt}, \quad (3.1)$$

where v_c represents the capacitor voltage and i_c refers to the capacitor current.

The capacitor voltage at time t_k can be derived from (3.1), which is given by

$$v_c(t_k) = v_c(t_{k-1}) + \frac{1}{C} \int_{t_{k-1}}^{t_k} i_c(\tau) d\tau. \quad (3.2)$$

When applying the Simpson quadrature method, (3.2) can be expressed as

$$v_c(t_k) = v_c(t_{k-1}) + \frac{\Delta t}{6C} \left[i_c(t_k) + 4i_c\left(\frac{t_k+t_{k-1}}{2}\right) + i_c(t_{k-1}) \right], \quad (3.3)$$

where $\Delta t = t_k - t_{k-1}$ is the simulation time step. $i_c\left(\frac{t_k+t_{k-1}}{2}\right)$ can be estimated by using the derivative of the capacitor current from last step, which is expressed as

$$i_c\left(\frac{t_k+t_{k-1}}{2}\right) = i_c(t_{k-1}) + \frac{i_c(t_{k-1}) - i_c(t_{k-2})}{2} = \frac{3i_c(t_{k-1}) - i_c(t_{k-2})}{2}, \quad (3.4)$$

3.2.2 Capacitor current

To solve capacitor voltages, capacitor currents must be determined, which depend on SM circuits and operating conditions. For the HB SM, the capacitor current can be derived as follows:

- Blocked condition: When the HB SM is blocked, the capacitor current is determined by the direction of the arm current and given by

$$i_c = \begin{cases} i_{\text{arm}} & , i_{\text{arm}} > 0, \\ 0 & , i_{\text{arm}} < 0. \end{cases} \quad (3.5)$$

- Normal condition: i_c depends on the insertion and bypass of the SM, and can be expressed as

$$i_c = S_{\text{SM}} i_{\text{arm}}, \quad (3.6)$$

where S_{SM} is the switching function of the HB SM and defined by

$$S_{\text{SM}} = \begin{cases} 1 & , \text{inserted}, \\ 0 & , \text{bypassed}. \end{cases} \quad (3.7)$$

For the fault-blocking SMs, under normal operating conditions, they behave like the HB SM and i_c can be determined by (3.6), in which S_{SM} is their corresponding switching states. Under fault operating conditions, for the UFB, FB, 3LCC, and 5LCC SMs, when all switches are turned off, either positive or negative arm currents through the anti-parallel diodes to charge the capacitors, and $i_c = |i_{\text{arm}}|$.

For the CD SM, under fault conditions, when the arm current is positive, two HB SMs in the CD SM are connected in series. When the arm current is negative, two HB SMs are connected in parallel. Therefore, when the CD SM is blocked, the capacitor currents can be calculated by

$$i_{c,1} = i_{c,2} = \begin{cases} |i_{\text{arm}}| & , i_{\text{arm}} > 0, \\ 0.5|i_{\text{arm}}| & , i_{\text{arm}} < 0, \end{cases} \quad (3.8)$$

where $i_{c,1}$ and $i_{c,2}$ are the currents of two capacitors in the CD SM, respectively.

For various SM configurations and operating conditions, when capacitor currents are determined and substituted into (3.3) and (3.4), the corresponding capacitor voltages can be solved.

3.2.3 Arm voltage

The voltage of the controllable voltage source of Fig. 3.1 can be calculated based on the number of the inserted SM capacitors. The number of the inserted SM capacitors is determined by SM circuits and switching states, arm current direction, and operating conditions.

Under normal operating conditions, various MMC configurations have similar behaviors. Both S1 and S4 of the proposed ECM are turned on and the arm voltage v_{arm} is determined by the number of the inserted SMs. For the CD, 3LCC, and 5LCC, two individual HB SMs are counted and controlled independently.

Under precharging and dc-fault conditions, for the HB-MMC, when the arm current is negative, $v_{arm} = 0$. When the arm current is positive, v_{arm} is the sum of the capacitor voltages of the off-state SMs. For the fault-blocking MMCs, v_{arm} is the sum of the capacitor voltages of the off-state SMs regardless of the direction of the arm current.

3.2.4 Implementation of the proposed detailed ECM

Figure 3.4 shows diagram of modeling the MMCs based on the proposed ECM. The system model includes the equivalent circuit of the MMC, control system, and voltage calculation. The operating condition is determined by the fault detection and the average capacitor voltage, which is listed in Table 3.2. The existing control strategies of the MMCs are applicable, which include the capacitor voltage balancing strategies, ac-side power/current control, circulating current control, and startup strategies. The gating signals and the arm currents are used to calculate capacitor voltages and arm voltages.

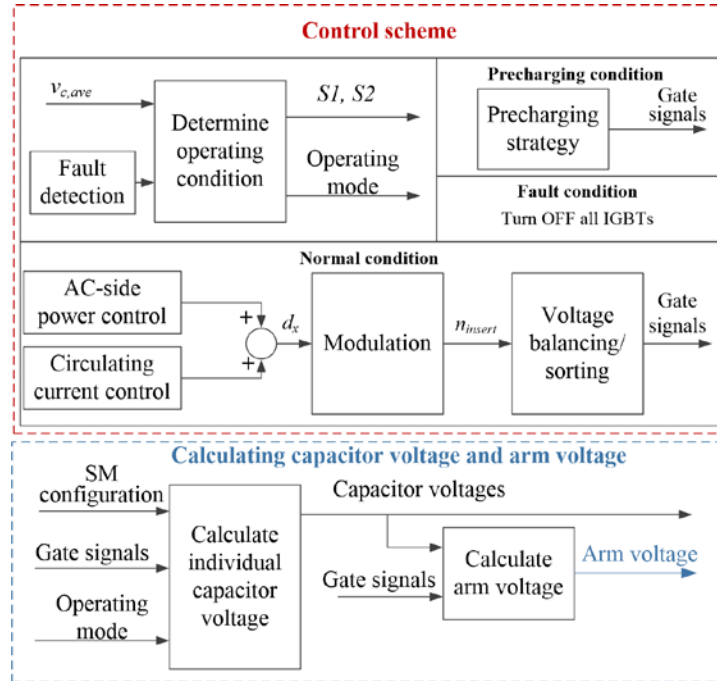


Figure 3.4 The block diagram of modeling the MMCs based on the proposed detailed ECM.

Table 3.2
Operating conditions of the MMCs

Fault detection	Capacitor voltage	Operating condition
Y	-	Fault
N	$V_{c,ave} < V_{threshold}$	Precharging
	$V_{c,ave} > V_{threshold}$	Normal

The proposed algorithm for calculating capacitor voltages and arm voltages is shown in Fig. 3.5.

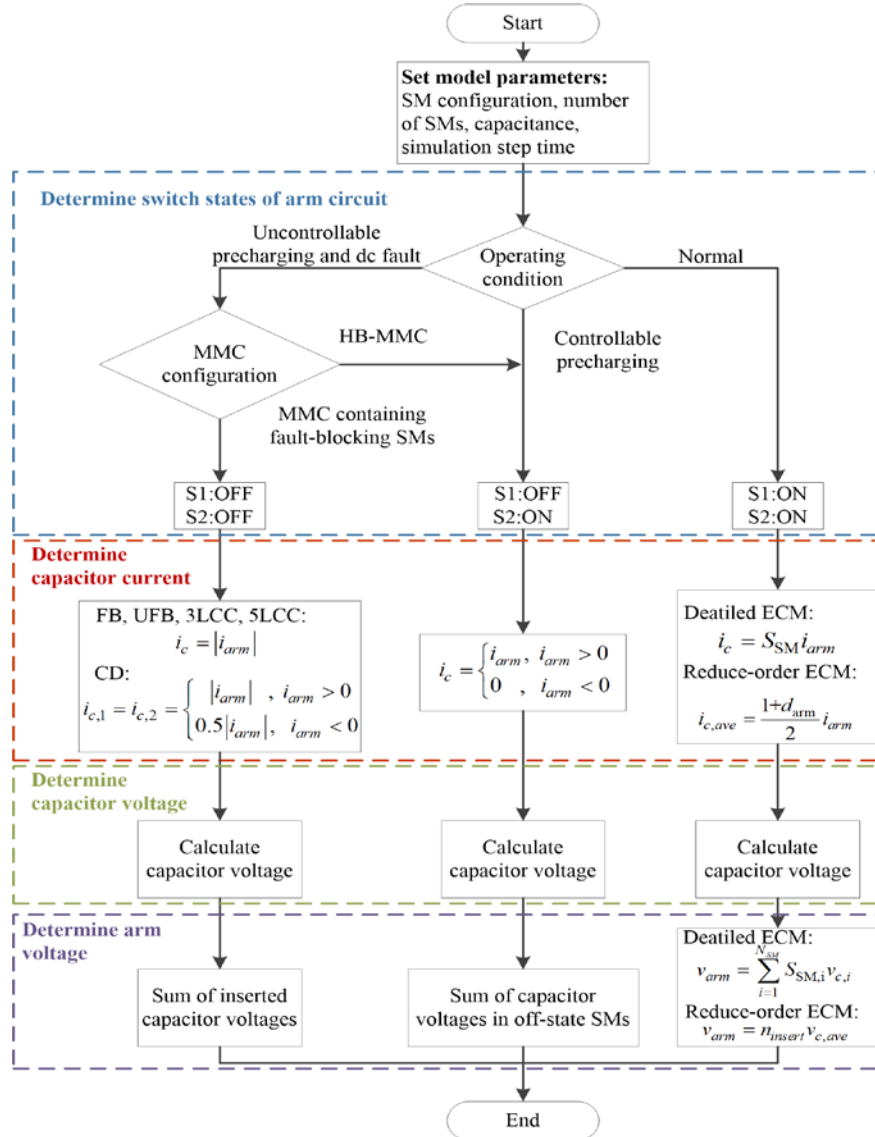


Figure 3.5 The flowchart of calculating capacitor voltages and arm voltages of the proposed ECM.

3.3 The Proposed Reduced-Order ECM

To further improve efficiency of modeling and simulating large-scale MMC-embedded hybrid ac and dc systems, the proposed ECM can be modified by reducing the number of state variables, i.e., capacitor voltages. This reduced-order ECM assumes that all capacitor voltages are well balanced and only the average capacitor voltage of each arm is considered to calculate the arm voltage.

3.3.1 Normal operating condition

Under normal operating condition, various SMs have similar operating behaviors. As analyzed in [23], the average capacitor current is derived as

$$i_{c,ave} = \frac{1+d_{arm}}{2} i_{arm} , \quad (3.9)$$

where d_{arm} is the duty cycle of each SM per arm, which is defined as $d_{arm} = m \cdot \sin(\omega t + \Phi_{arm})$. The average capacitor voltage of an arm can be derived by (3.3) and (3.9). The arm voltage is determined by the number of the inserted SM capacitors, which is given by:

$$v_{arm} = n_{insert} v_{c,ave} , \quad (3.10)$$

where n_{insert} is the number of the inserted capacitors, and $v_{c,ave}$ is the average SM capacitor voltage of an arm.

3.3.2 Precharging and dc fault conditions

Under uncontrollable precharging and dc fault conditions, the capacitor currents of various SMs are governed by (3.5) and (3.8). The arm voltage is determined by the SM configuration and the number of capacitors.

Under the controllable precharging condition, for the reduced-order ECM, the switching function is unavailable. The average capacitor voltage is determined by the equivalent capacitance per arm, which is determined by the SM configurations and the number of inserted capacitors and analyzed in [19].

3.3.3 Implementation of the proposed reduced-order ECM

For the reduced-order ECM, the system model can be simplified by removing the voltage balancing strategy, as shown in Fig. 3.6. The modulation generates the number of the inserted SMs rather than generating the gating signals. To calculate the average capacitor voltage and the arm voltages, the algorithm of Fig. 3.5 is applied.

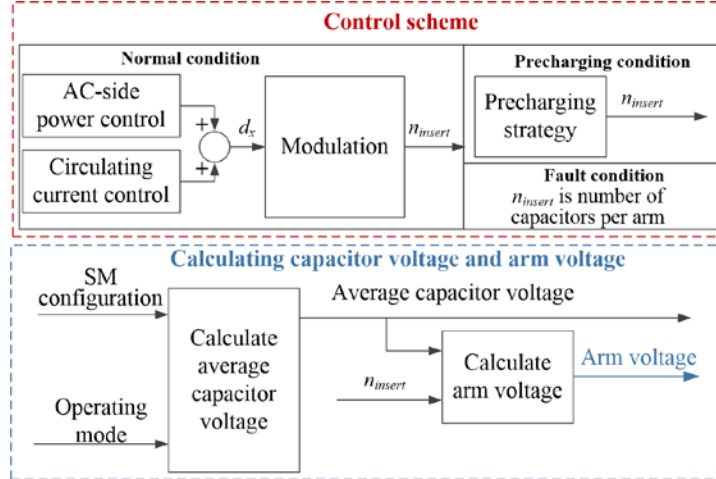


Figure 3.6 The block diagram of modeling the MMCs based on the proposed reduce-order ECM.

4. Simulation Verification

To verify the proposed ECM, a point-to-point MMC-HVDC system is selected as the study system and built in PSCAD/EMTDC program environment, as shown in Fig. 4.1. The system parameters are listed in Table 4.1.

Table 4.1
System parameters of the MMC-HVDC system

Parameters	Nominal value
Rated power	100 MW
DC link voltage	100 kV
AC grid line-line voltage	60 kV RMS
Number of SMs per arm, N_{SM}	20
Arm inductance	5 mH
Capacitance per SM	1000 μ F
Rated capacitor voltage per SM	5 kV
DC line inductance	1 mH
DC line resistance	1 Ω
DC line capacitance	100 μ F

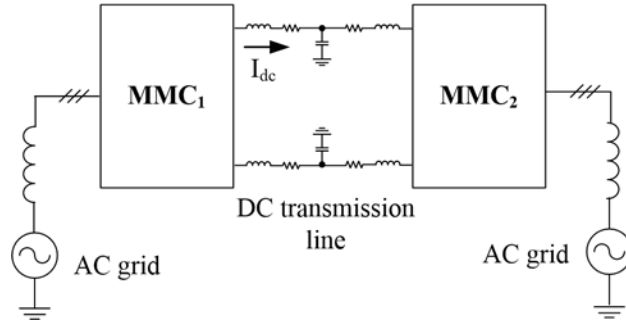


Figure 4.1 The schematic diagram of a point-to-point MMC-HVDC system.

4.1 The Proposed Detailed ECM

- HB-MMC: The HB-MMC-HVDC system is modeled and simulated based on the DSM and the proposed detailed ECM, respectively. Their phase-a arm currents, dc currents, and capacitor voltages are compared, which coincide and demonstrate the accuracy of the proposed ECM, as shown in Fig. 4.2. During 0.6 to 0.7 s, when dc fault occurs, the HB-MMC cannot block the fault current fed from ac grid. As shown in Fig. 4.2, the waveforms of arm currents and capacitor voltages generated by the DSM and the proposed detailed ECM coincide, which demonstrate the accuracy of the proposed ECM under normal and fault conditions.

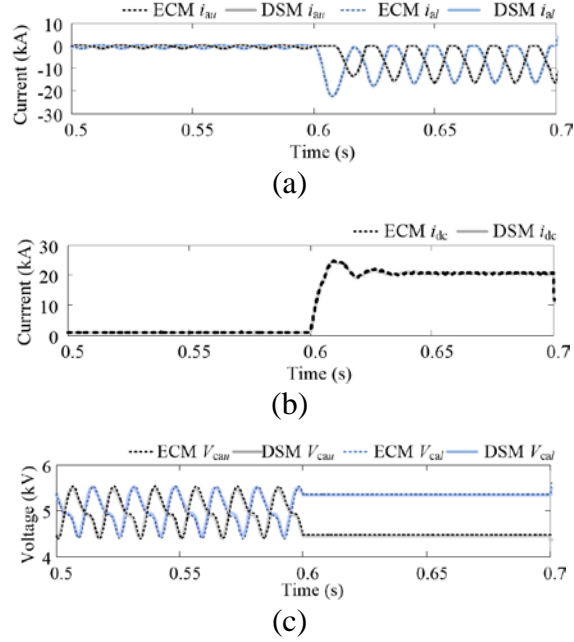


Figure 4.2 The simulation results of the HB-MMC-HVDC based on the DSM and the proposed detailed ECM: (a) phase current, (b) dc current, and (c) capacitor voltage.

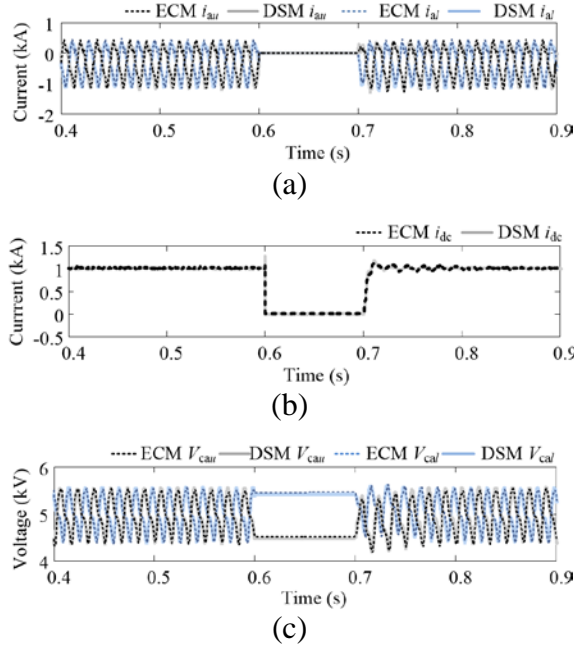


Figure 4.3 The simulation results of the FB-MMC-HVDC based on the DSM and the proposed detailed ECM: (a) phase current, (b) dc current, and (c) capacitor voltage.

- FB-MMC: FB-MMC: The MMCs based on the FB, UFB, 3LCC, and 5LCC SMs have the similar behaviors. Figures 4.3 shows the phase-a arm currents, dc current, and capacitor voltages of the FB-MMC-HVDC system modeled by the DSM and the proposed detailed ECM, respectively. Figure 4.4 shows the capacitor voltages based on

the DSM and the proposed detailed ECM under different operating conditions, which demonstrates that the proposed ECM can effectively model and simulate the MMC-based systems for various operating conditions.

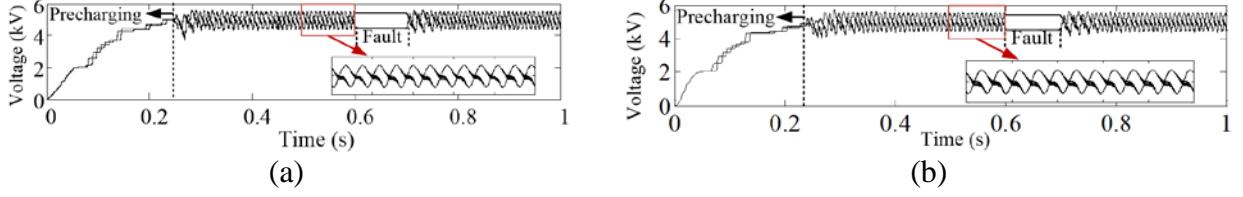


Figure 4.4 The capacitor voltages of MMC1 of the FB-MMC-HVDC based on: (a) the DSM, and (b) the proposed detailed ECM.

- Fault-STATCOM operation of the FB-MMC: Under dc-fault condition, the FB-MMC can operate as a STATCOM to compensate reactive power for ac grid. The corresponding simulation results of the DSM and detailed ECM are shown in Fig. 4.5.

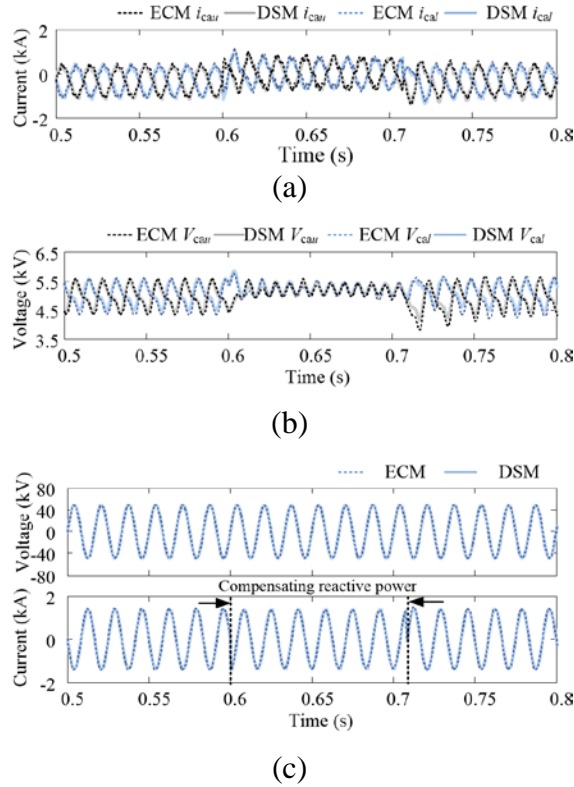


Figure 4.5 The simulation results of the FB-MMC operating as a STATCOM: (a) capacitor voltages, (b) phase-a arm currents, and (c) ac-side phase current and voltage.

4.2 The Proposed Reduced-order ECM

If capacitor voltage balancing strategies are not considered, the proposed detailed ECM can be simplified by assuming that all capacitor voltages are balanced well. This reduced-order ECM

has better simulation efficiency by considering the average capacitor voltage and neglecting the dynamics of each capacitor voltage.

- HB-MMC: The phase-a arm currents and capacitor voltages of the HB-MMC based on the reduced-order ECM are compared with those of the HB-MMC based on the DSM and shown in Fig. 4.6.

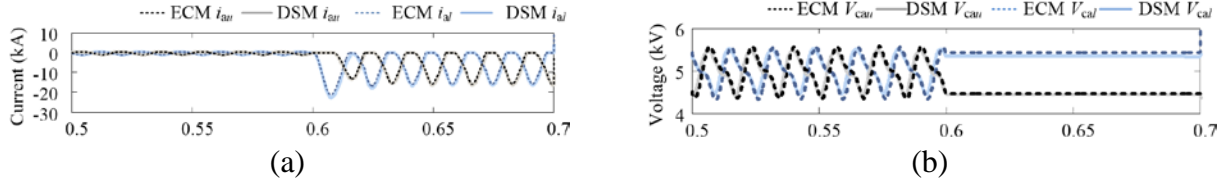


Figure 4.6 The simulation results of MMC1 of the HB-MMC-HVDC based on the DSM and the proposed reduced-order ECM: (a) arm currents, and (b) capacitor voltages.

- FB-MMC: For the FB-MMC-HVDC, the arm currents, dc current and capacitor voltages under various operating conditions are shown in Fig. 4.7, which demonstrate the effectiveness of the proposed reduced-order ECM. Based on the simulation results, the arm currents and capacitor voltages coincide and the proposed reduced-order ECM is applicable for various operating conditions.

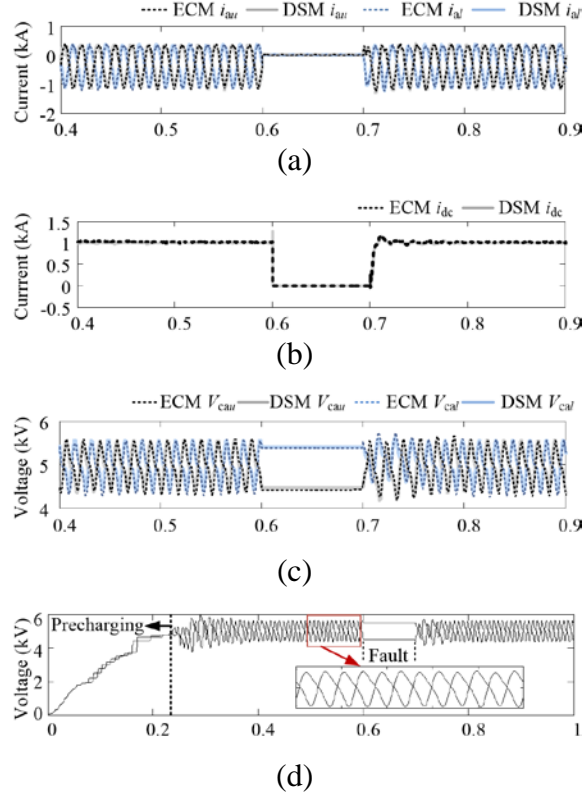


Figure 4.7 The simulation results of MMC1 of the FB-MMC-HVDC based on the DSM and the proposed reduced-order ECM: (a) arm currents, (b) dc current, (c) and (d) capacitor voltages.

- Fault-STATCOM of FB-MMC: Under dc-fault condition, the FB-MMC can operate as a STATCOM to compensate reactive power for ac grid. The corresponding simulation results of the DSM and reduced-order ECM are shown in Fig. 4.8.

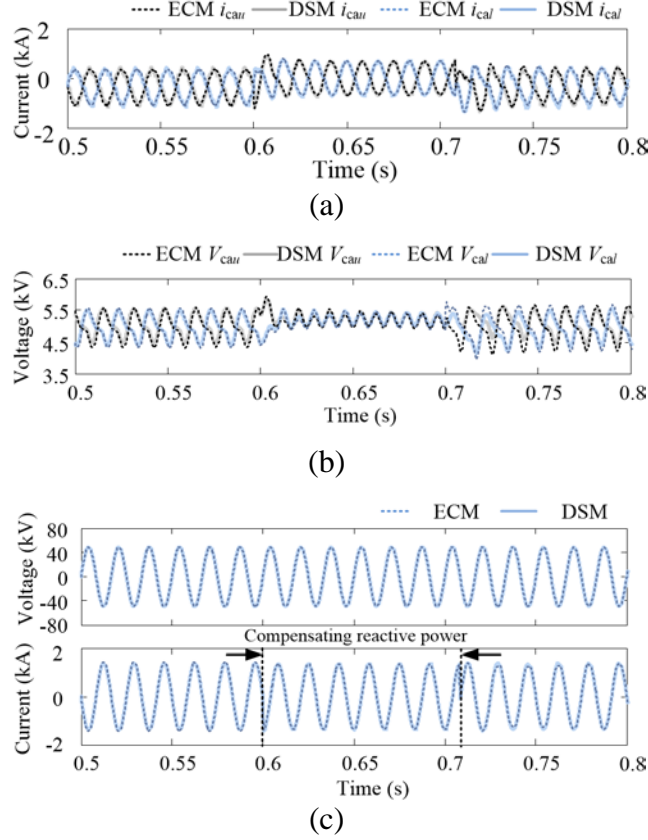


Figure 4.8 The capacitor voltages of the FB-MMC based on the reduced-order ECM operates as a STATCOM: (a) capacitor voltages, (b) arm currents, and (c) ac-side phase current and voltage.

4.3 Computational Efficiency

4.3.1 The MMC-HVDC systems based on various SM circuits

To evaluate the efficiency of the proposed ECM, the simulation speed for various MMC-HVDC systems based on the DSM, the detailed ECM, and the reduced-order ECM is listed in Table 4.2. The system operating time is 1 s and the simulation time step is 10 μ s. The simulations are conducted on the operating system of Microsoft Windows 10 with a 2.60 GHz Intel Core i7-6700HQ CPU and 8 GB of RAM. Based on the study results shown in Table 4.2, the simulation run time can be reduced from several or tens of thousands seconds to tens of seconds. For the conventional DSM, the SMs with more complex circuit topology have longer runtime. However, by using the proposed ECM, the run time is not related to the complexity of SM circuit topology.

Table 4.2
Comparison of simulation speed (run time) for various MMC-HVDC
systems based on the DSM and the proposed ECM

Simulation settings			
Simulation time step = 10 μ s ; System operating time = 1 s.			
MMC configuration	DSM (s)	ECM (s)	
		Detailed	Reduced-order
HB	1656.21	30.67	11.52
FB	8512.72	31.34	11.73
CD	21877.39	30.31	12.38
3LCC	29097.14	30.84	12.21
Hybrid (HB and FB)	3179.83	30.56	11.94

4.3.2 The high-level MMC-HVDC systems

Table 4.3 shows the simulation speed for the MMC-HVDC systems with various voltage levels. As the increasing of the number of SMs, although the simulation speed of the proposed ECM becomes slow, it still much faster than that of the conventional DSM.

Table 4.3
Comparison of simulation speed (run time) for various MMC-HVDC
systems with different voltage levels

MMC Levels	ECM (s)		DC voltage (kV)
	Detailed	Reduced-order	
21	31.34	11.73	100
41	37.11	12.03	120
61	43.89	12.45	180
81	47.80	12.71	240
101	54.62	13.12	300
201	96.56	16.29	600

Based on Table 4.3, the run time of the proposed ECM increases with the increasing number of voltage levels. For the proposed reduced-order ECM, there is no significant increase in run time when the voltage level is low.

5. Conclusions

In this project, by studying the behaviors of various SM circuits, a generalized arm equivalent circuit is proposed to model and simulate various arm behaviors under startup/precharging, normal, and fault conditions. Based on the proposed equivalent arm circuit, the detailed equivalent circuit model (ECM) of MMC is developed, which considers all internal states and can be used to investigate internal dynamic control strategies, e.g., capacitor voltage balancing strategies. To further improve simulation efficiency, the reduced-order ECM is derived by neglecting the dynamics of individual capacitor voltage and considering the average capacitor voltage. The proposed modeling technique is applied to an MMC-HVDC system and compared with the conventional DSM to verify simulation efficiency and accuracy. Based on the simulation results, the following conclusions are obtained.

- The proposed ECM can significantly improve simulation efficiency (speed) while keeping enough accuracy.
- The complexity of SM circuit topology significantly influences the simulation run time for the conventional detailed switching model. However, there is no significant impact of SM circuit topology on the run time of the proposed ECM.
- The run time of the proposed ECM increases with the increasing to the number of voltage levels.

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